

Compal Confidential

PAU30 M/B Schematics Document

Intel Arrandale Processo SV with DDRIII + Ibex Peak-M



PCB PAU30 LA-6392P LS-6391P/6392P/6393P/6394P



PCB 0F9 LA-6392P REV1 M/B



PCB 0F9 LS-6391P REV1 POWER_BTN/B



PCB 0F9 LS-6392P REV1 SWITCH/B



PCB 0F9 LS-6393P REV1 LED/B



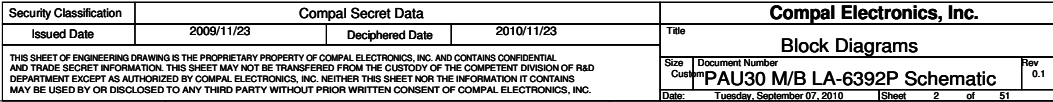
PCB 0F9 LS-6394P REV1 LID SWITCH/B

2010-11-22

REV:1.0

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Model Name : PAU30
File Name : LA-6392P



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for Arrandale GPU (only for arrandaleCPU)	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for ARD CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

43level BOM Config

P/N	Des.	BOM Config
431954BOL01	SMT MB A6392 PAU30 W/3G	DAZ@

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

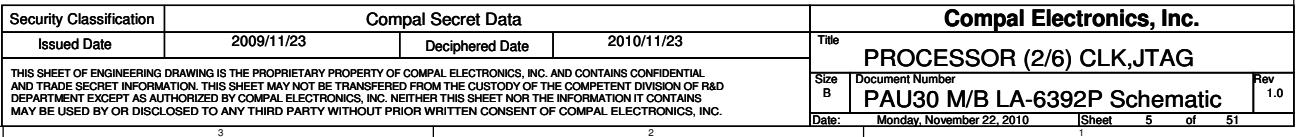
BTO Option Table

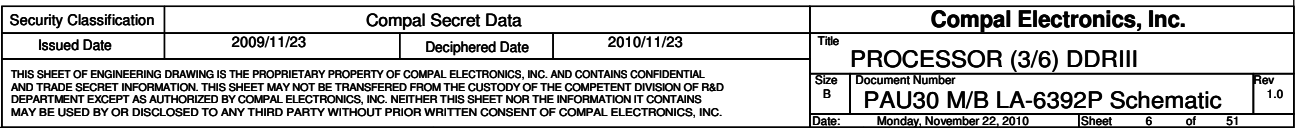
BTO Item	BOM Structure
VRAM	
VRAM	X76@
Connector	CONN@
Ventura	VENTURA@
Blue Tooth	BT@
Unpop	@

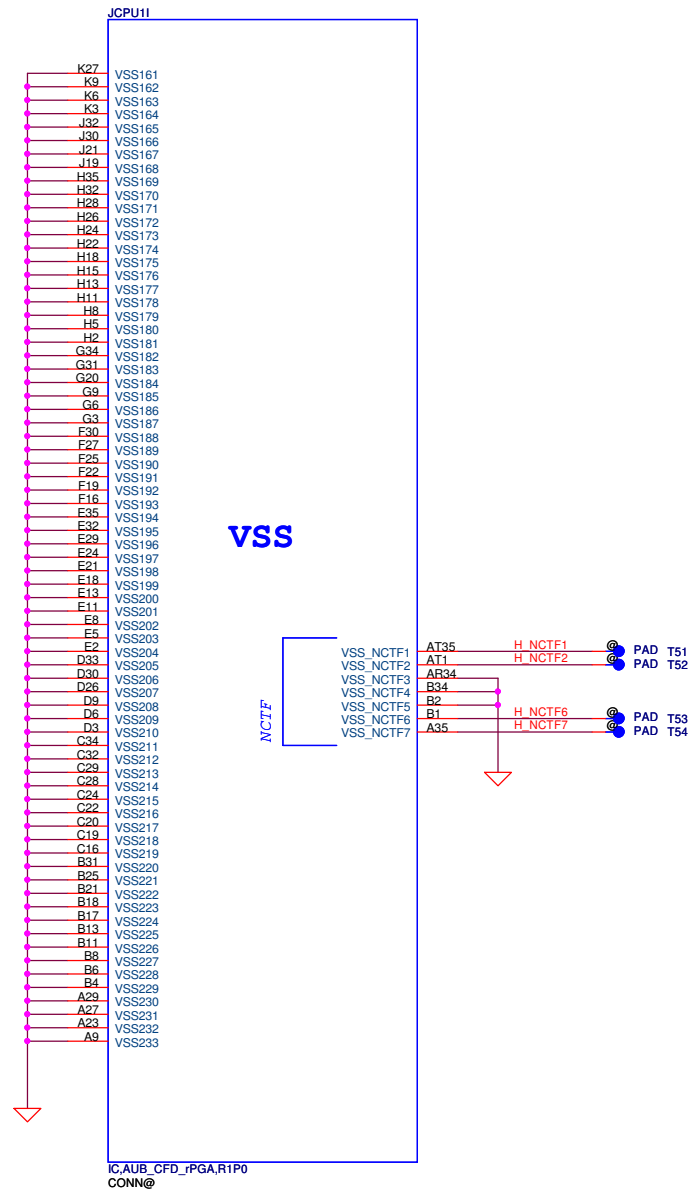
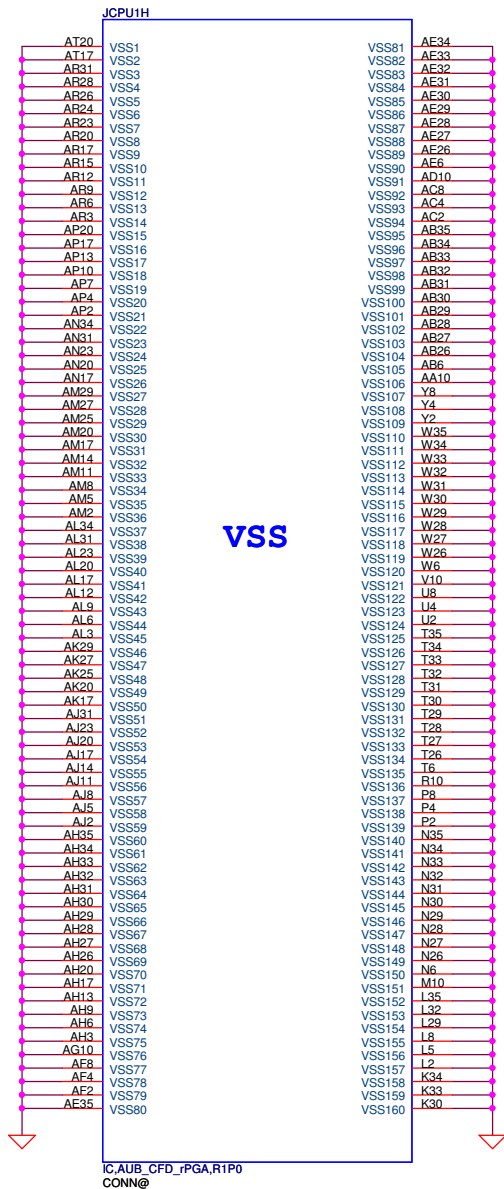
USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB Port (Left Side)
		1	USB Port (Left Side)
	UHCI1	2	USB/Touch Screen2
		3	USB/Touch Screen1
	UHCI2	4	Mini Card(WLAN)
		5	SIMM CARD
	UHCI3	6	
7			
EHCI2	UHCI4	8	Camera
		9	Mini Card(3G)
	UHCI5	10	
		11	
	UHCI6	12	
		13	Blue Tooth

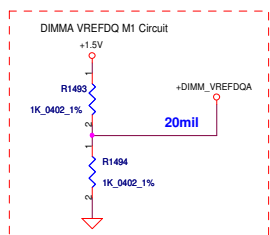
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Size B	Document Number			Rev	
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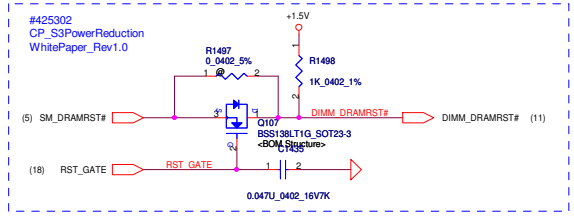
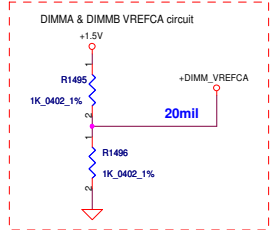




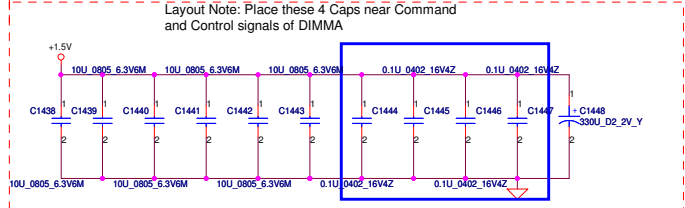
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								PROCESSOR (6/6) VSS							
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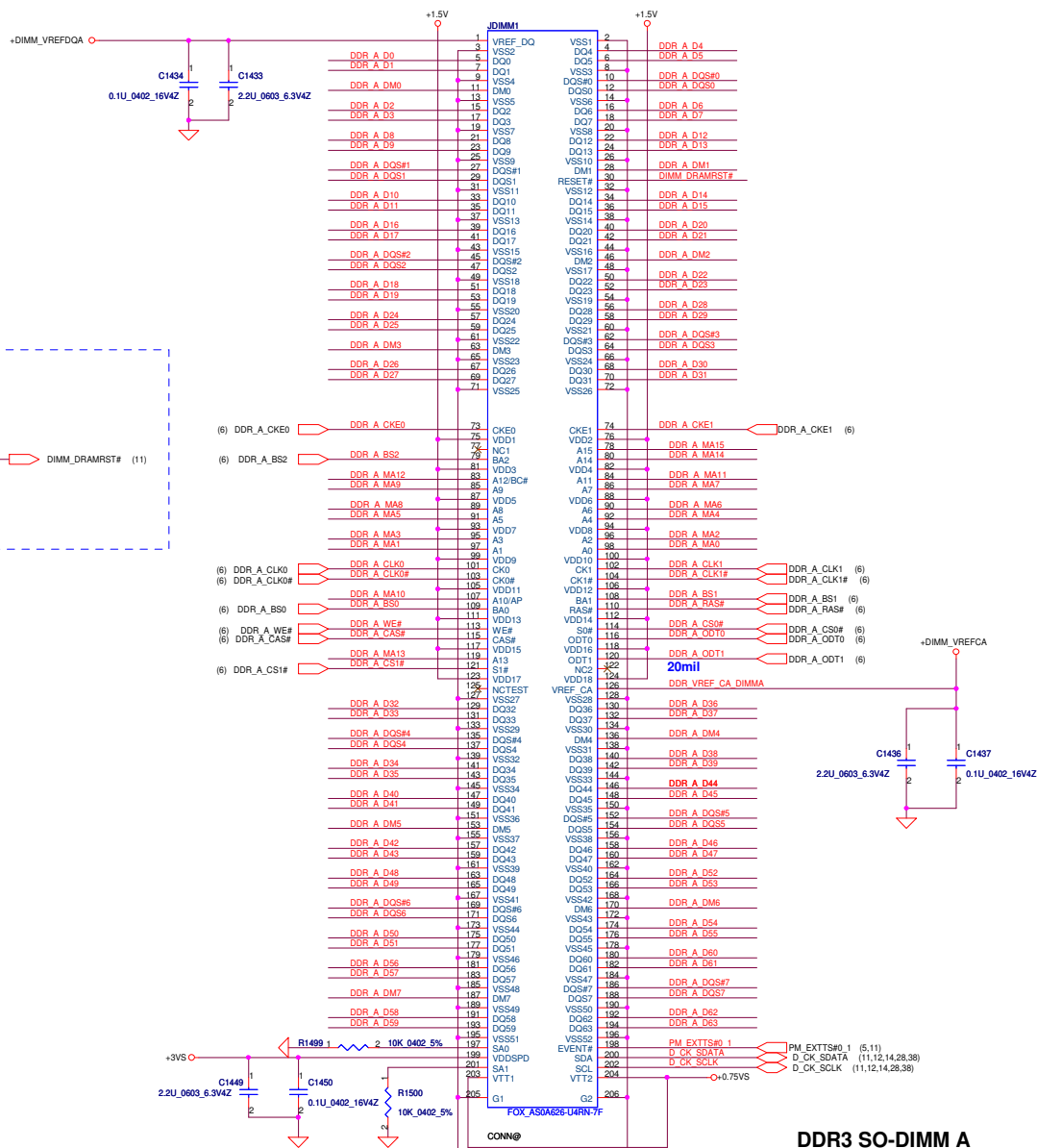
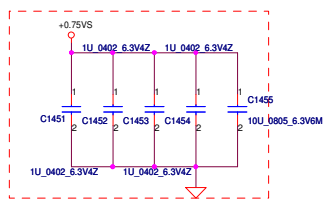
- (6) DDR_A_DQS#0..7
- (6) DDR_A_DQ#0..63
- (6) DDR_A_DM#0..7
- (6) DDR_A_DQS#8..15
- (6) DDR_A_MA#0..15



Layout Note:
Place near JDIMM1

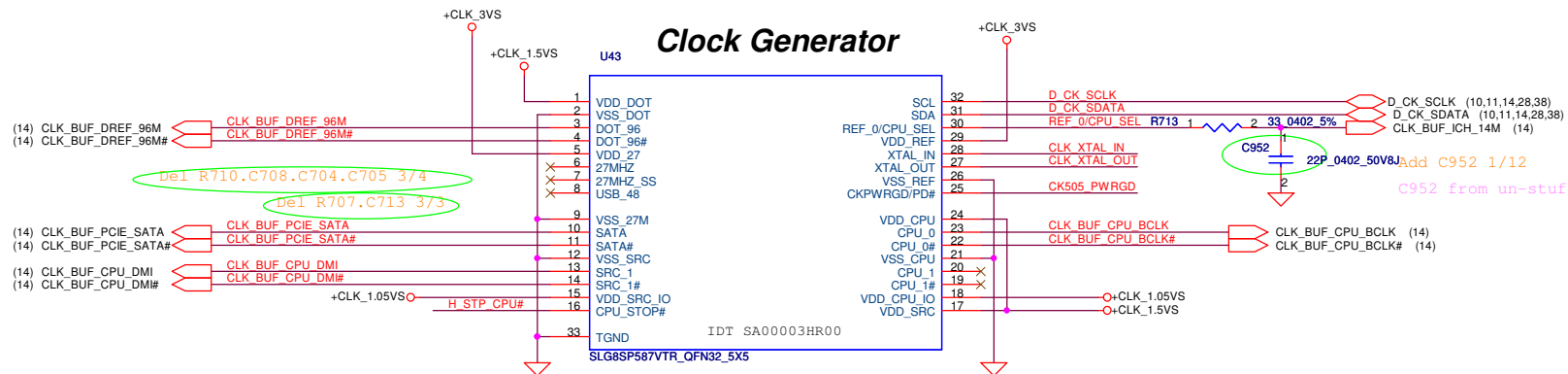
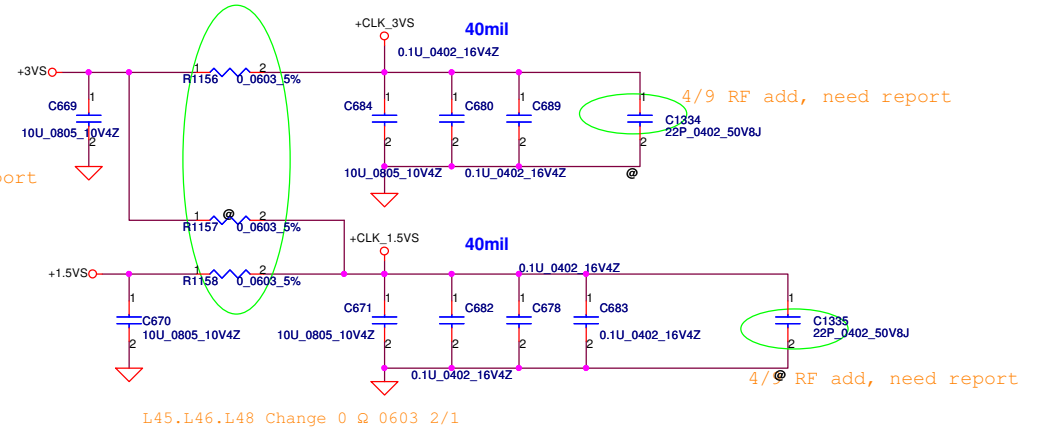
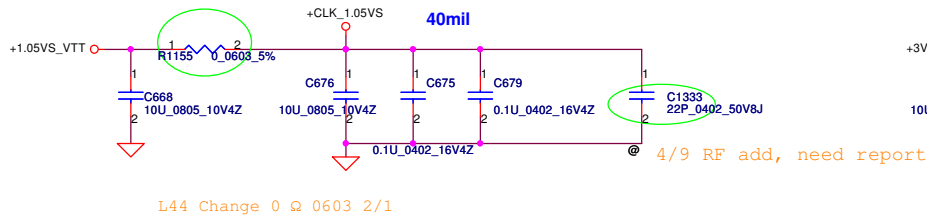


Layout Note:
Place near JDIMM1.203 & JDIMM1.204

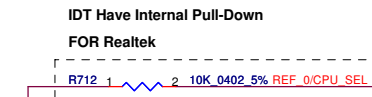
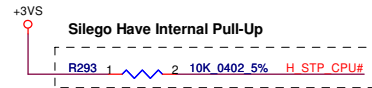


DDR3 SO-DIMM A
H=8mm

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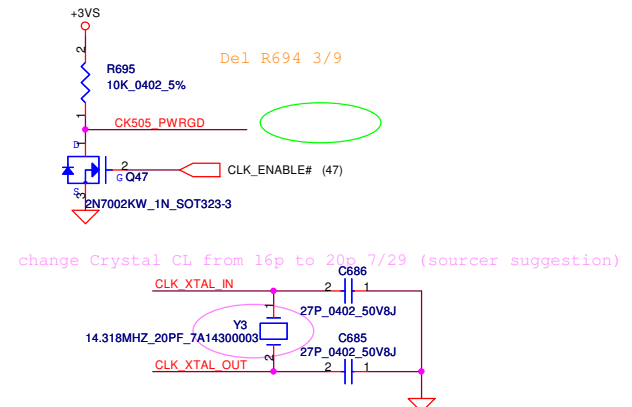


Low Power:
 IDT: 9LVS3199AKLFT, SA00003HR00
 Realtek: RTM890N-631-GRT, SA00003HQ00
 Silago: SLG8LV597VTR, SA00003MF00

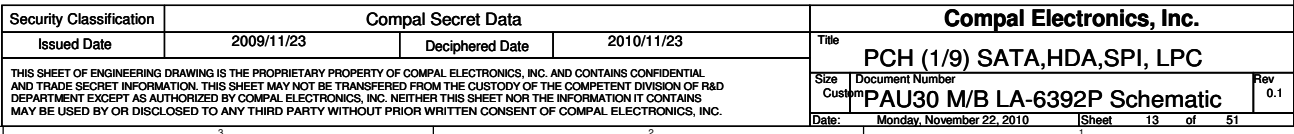


PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

Move Q50 and Q51 to PCH Side 1/12



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For PCIE LAN

For Wireless LAN

Add for USB30 3/1
For USB3.0

For 3G/GPS MiniCard

For PCIE LAN

For Wireless LAN

Del R647,R646,Q39 1/7

Del PCH-GPIO18 off page 1/8

Change Netname From MINI1_CLKREQ# to PCH_GPIO18 1/12

Del PCH_GPIO20 off page 1/8

Add R1244 for USB30 3/1

Del Q39.R647 3/12

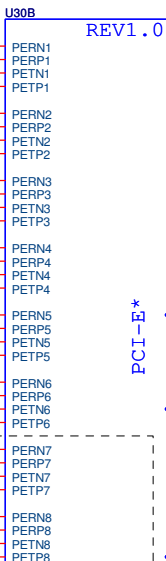
Move R208 to MINI1 Side 3/18

Move R638 to MINI2 Side 3/18

(28) MINI2_CLKREQ#

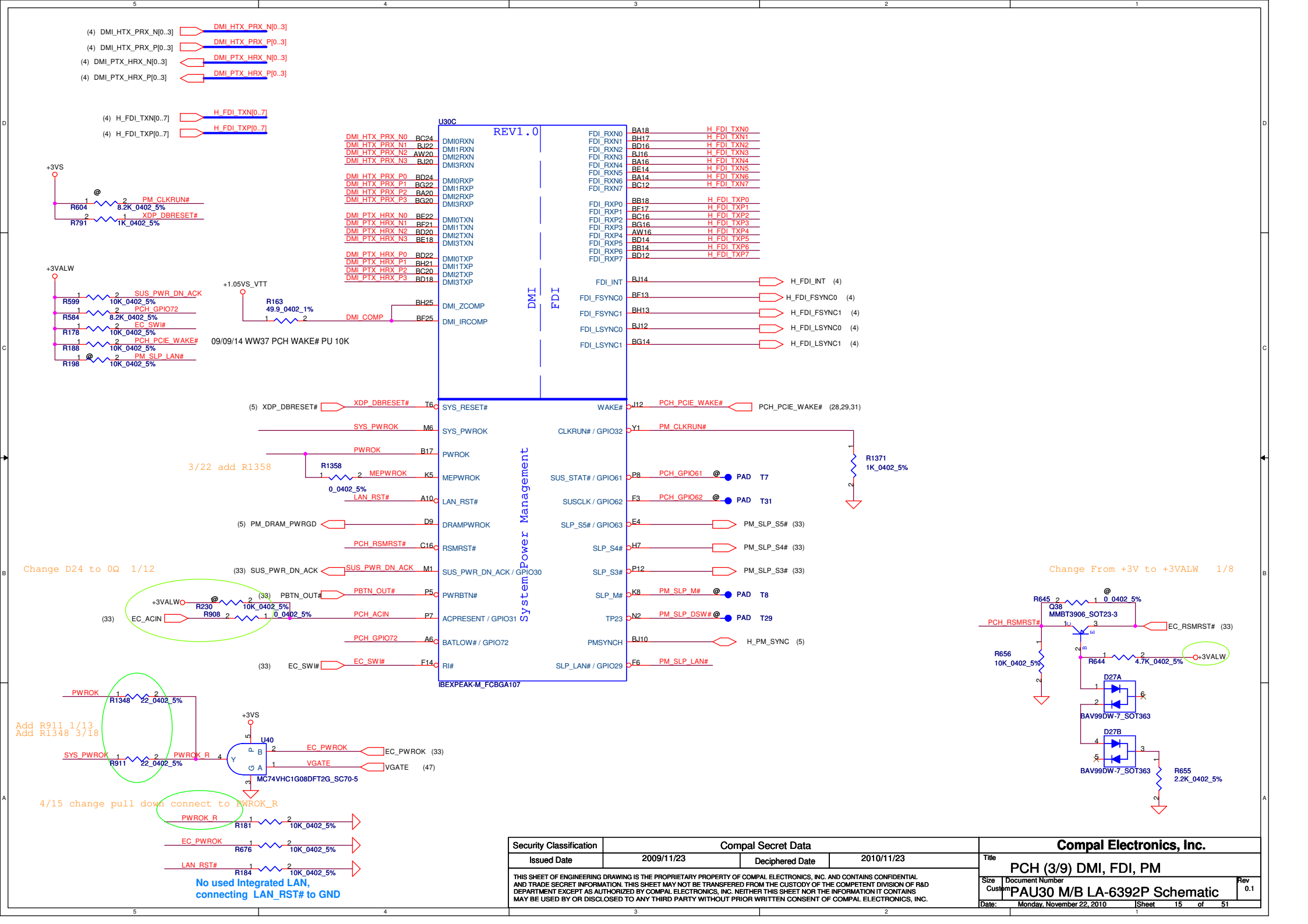
MINI1_CLKREQ# R227 1 2 10K 0402 5%
PCH_GPIO20 R622 1 2 10K 0402 5%

PCH_SMBCLK R173 1 2 4.7K 0402 5%
PCH_SMBDATA R582 1 2 4.7K 0402 5%
PCH_GPIO60 R169 1 2 10K 0402 5%
PCH_SML1CLK R191 1 2 3.3K 0402 5%
PCH_SML1DAT R183 1 2 3.3K 0402 5%
PCH_GPIO74 R214 1 2 10K 0402 5%
PCH_GPIO44 R190 1 2 10K 0402 5%
PCH_GPIO56 R211 1 2 10K 0402 5%

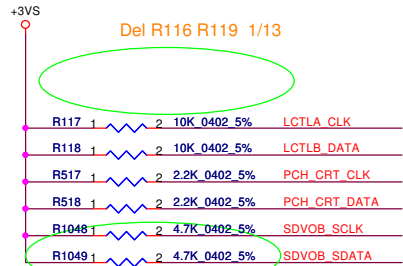


	RAM ID0	ID1	ID2	ID3
	GPIO66	GPIO65	GPIO21	GPIO19
H	Samsung	256MX8	2 channel	Reserved*
L	Hynix	128MX8	1 channel	Reserved

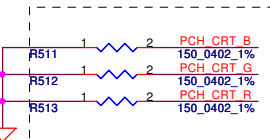
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IGPU_BKLT_EN Pull down 100K at EC Side
PCH_ENVDD Pull down 100k at JLVDS1 Side
PCH_LCD_CLK and PCH_LCD_DATA Pull high 4.7K at JLVDS1 Side

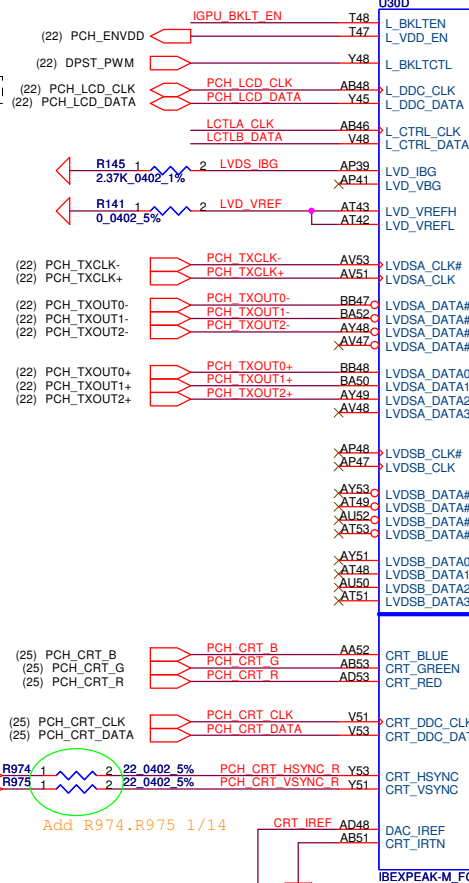


Change R1048.R1049 From 2.2KQ to 4.7KQ 1/18



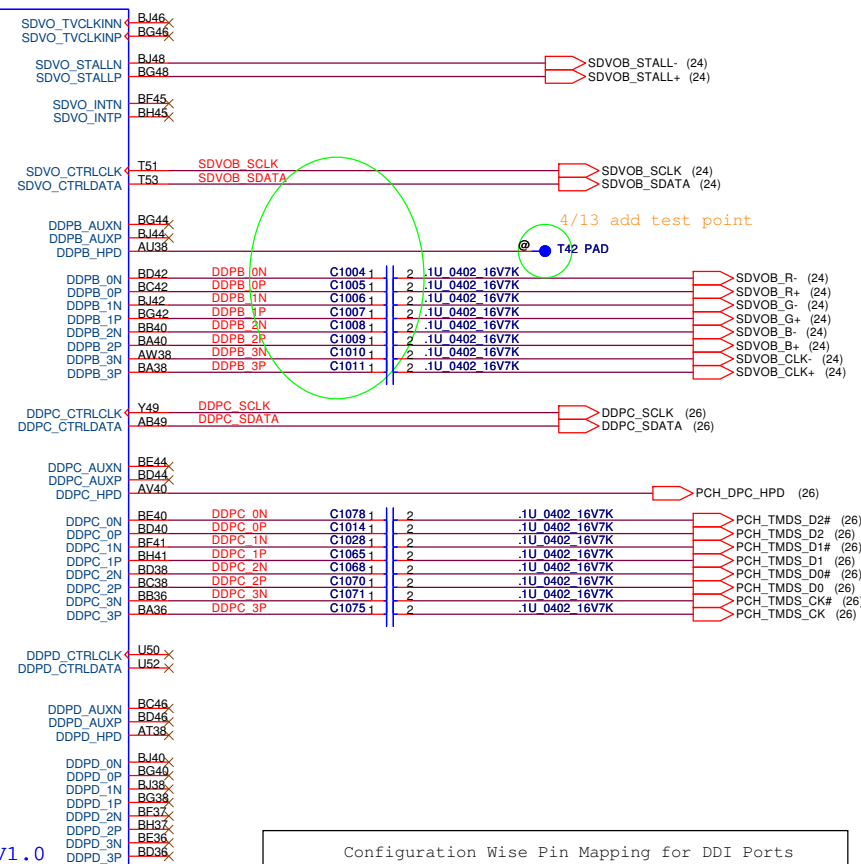
(33) ENBKL ENBKL R112 1 2 0 0402 5% IGPU_BKLT_EN

Del U11.C230.R115.R126 1/7



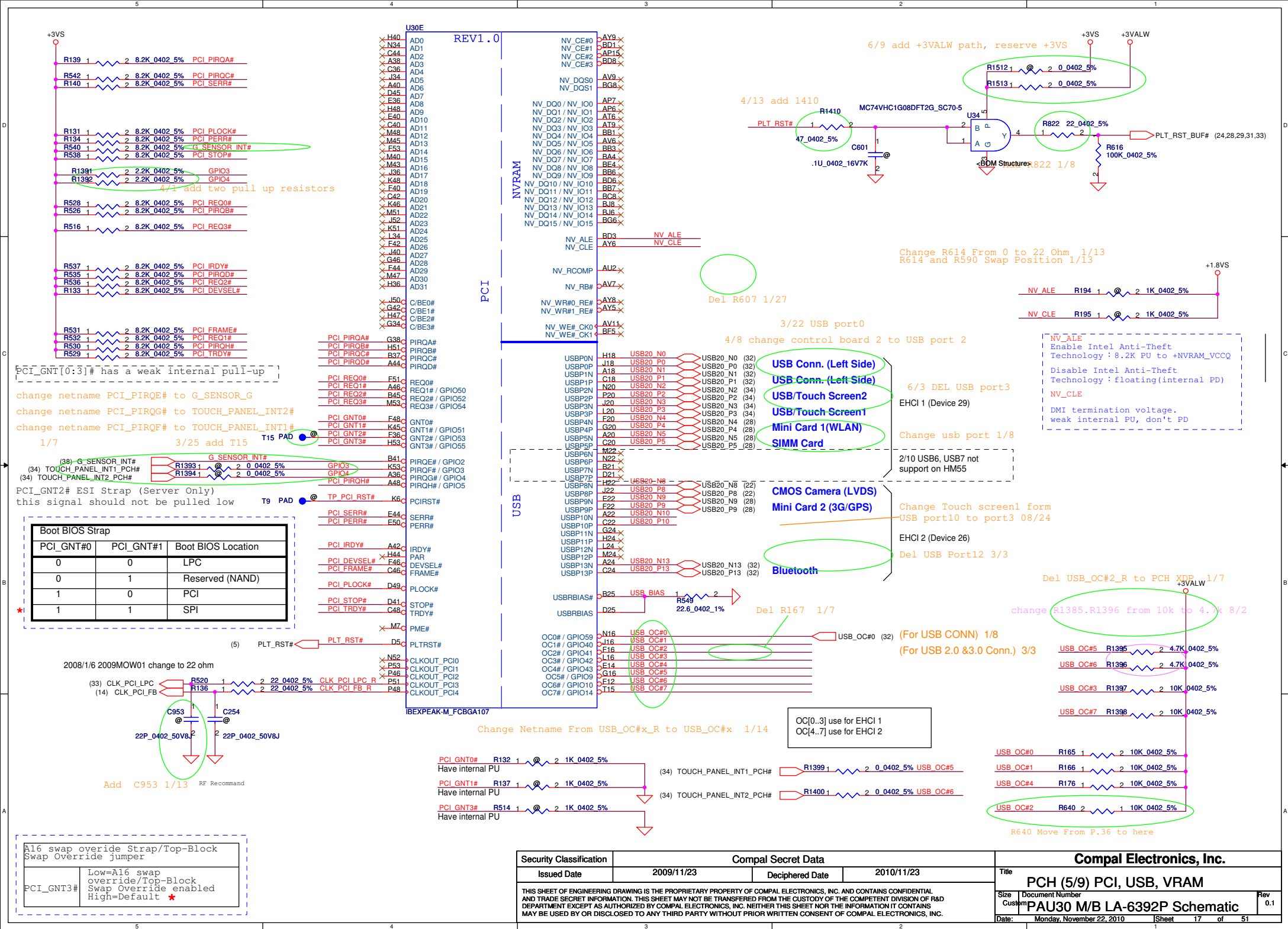
Digital Display Interface

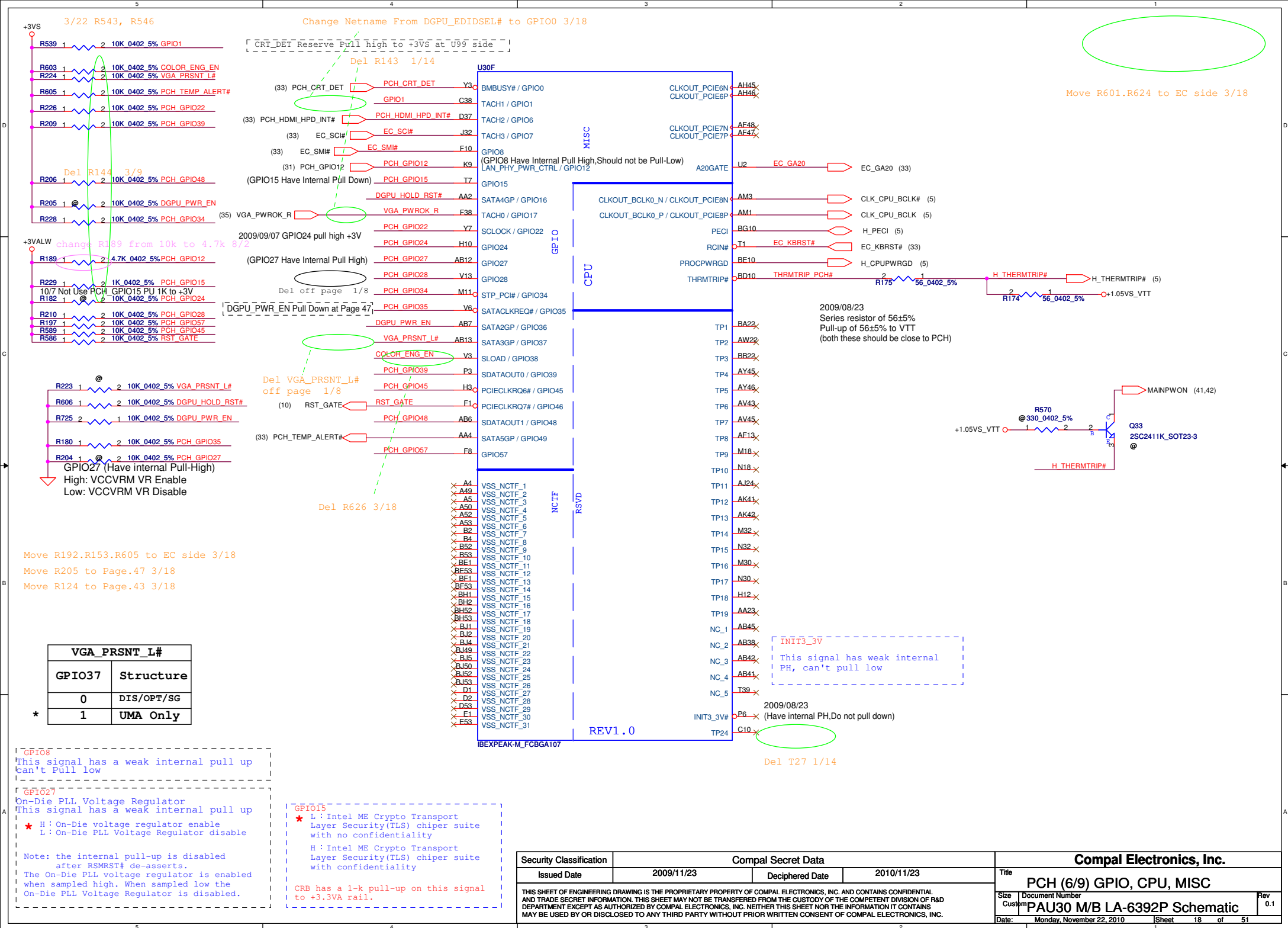
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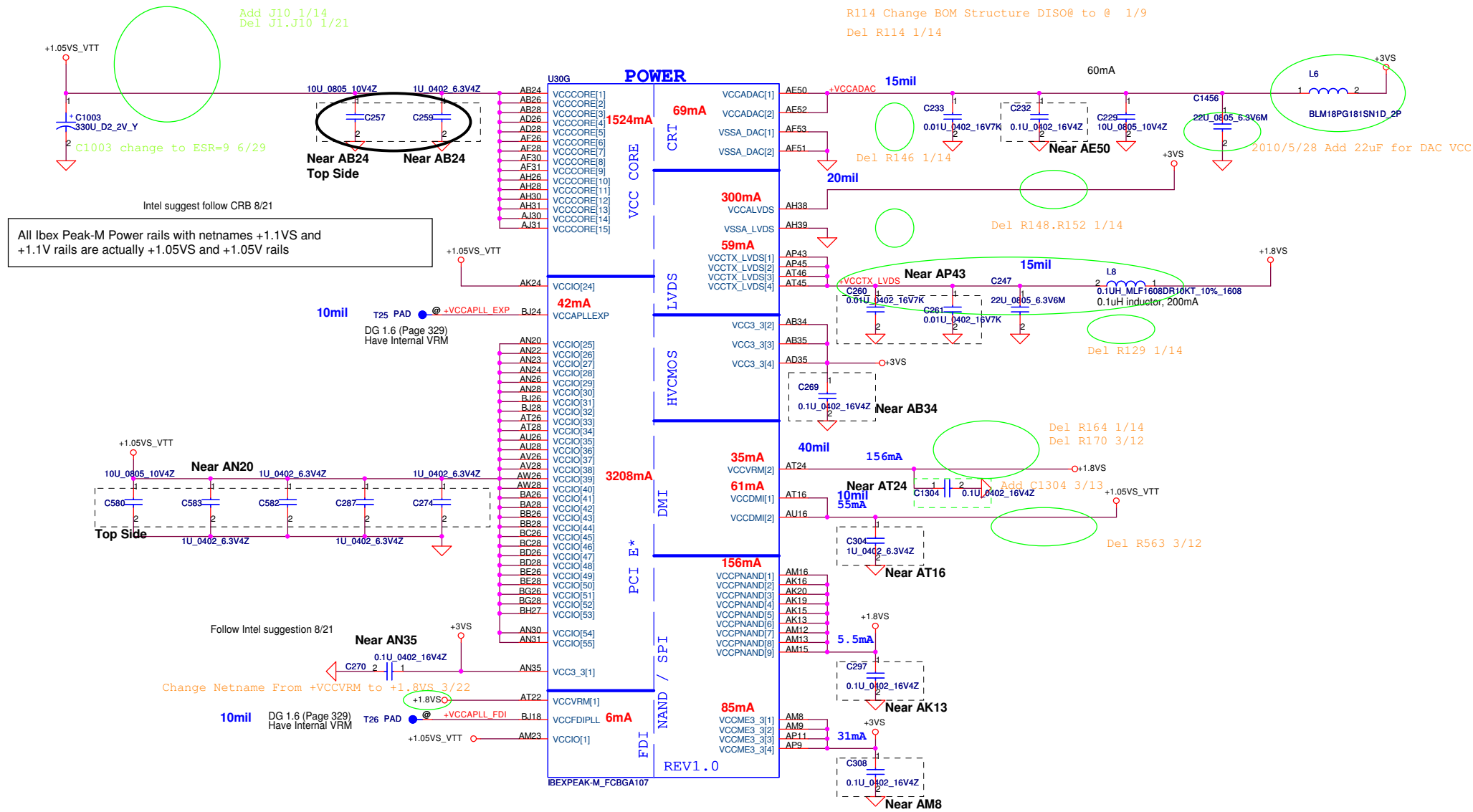


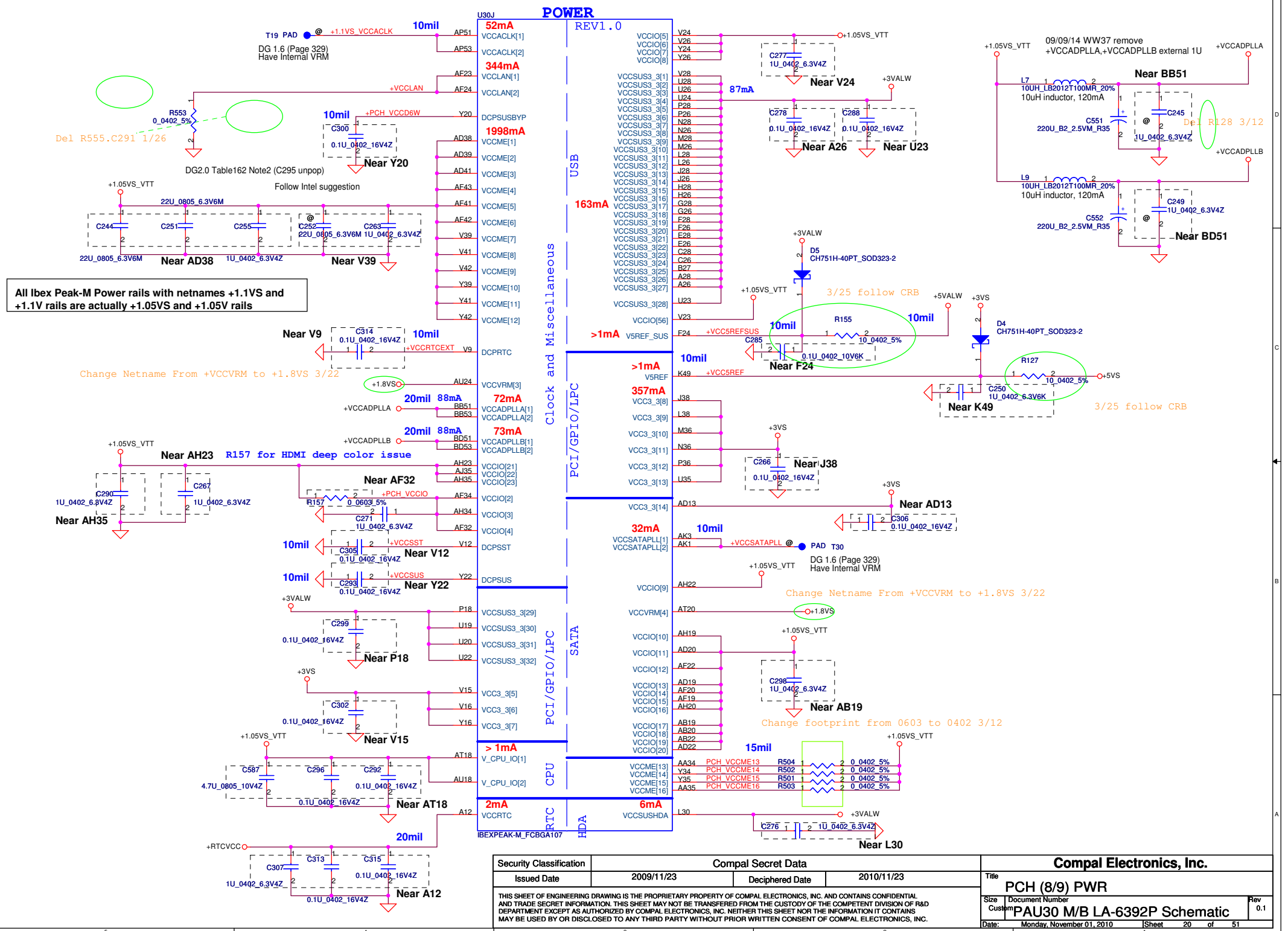
Configuration Wise Pin Mapping for DDI Ports

DDI PCH Pin Names	SDVO Mapping	HDMI/DVI Mapping	DisplayPort Mapping
DDPB_0]P	SDVO_RED	TMDSB_DATA2	DDPB_0]P
DDPB_0]N	SDVO_RED#	TMDSB_DATA2#	DDPB_0]N
DDPB_1]P	SDVO_GREEN	TMDSB_DATA1	DDPB_1]P
DDPB_1]N	SDVO_GREEN#	TMDSB_DATA1#	DDPB_1]N
DDPB_2]P	SDVO_BLUE	TMDSB_DATA0	DDPB_2]P
DDPB_2]N	SDVO_BLUE#	TMDSB_DATA0#	DDPB_2]N
DDPB_3]P	SDVO_CLK	TMDSB_CLK	DDPB_3]P
DDPB_3]N	SDVO_CLK#	TMDSB_CLK#	DDPB_3]N
DDPB_AUXP	NA	NA	DDPB_AUXP
DDPB_AUXN	NA	NA	DDPB_AUXN
DDPB_HPD	NA	HDMI_HPD	DDPB_HPD
SDVO_CTRLCLK	SDVO_CTRLCLK	HDMI_CTRLCLK	NA
SDVO_CTRLDATA	SDVO_CTRLDATA	HDMI_CTRLDATA	NA

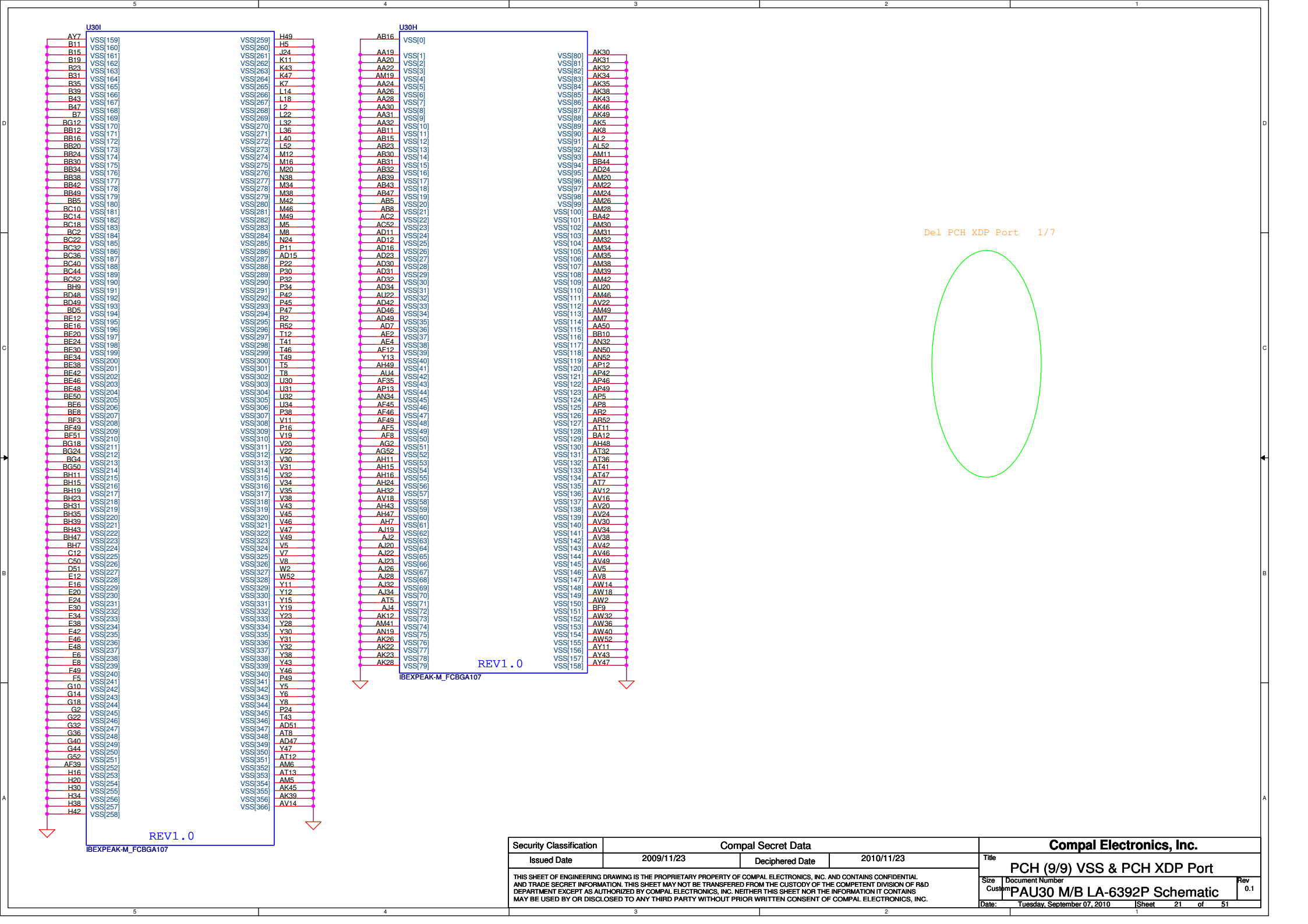






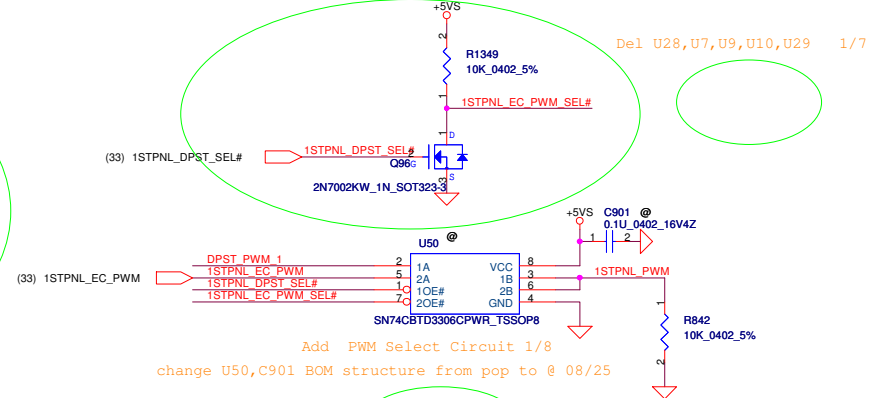


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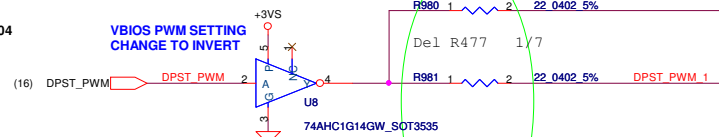
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Change 1STPNL_DPST_SEL# Circuit 3/18

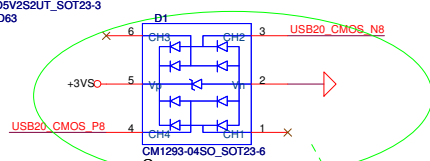


change U50,C901 BOM structure from pop to @ 08/25

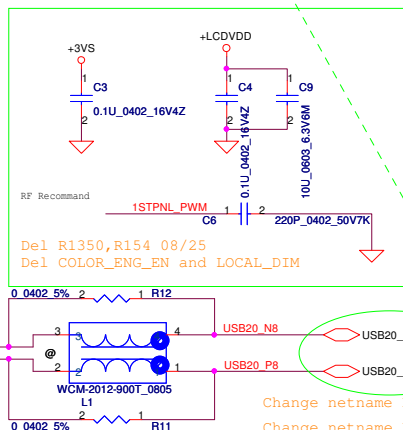
2009/09/08
change P/N to SA741140100



```
add JLVDS3 08/26
modify JLVDS3 pin define 08/27
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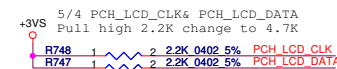


Del C1.C2.C5 3/12



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Del R1350,R154 08/25
Del COLOR_ENG_EN and
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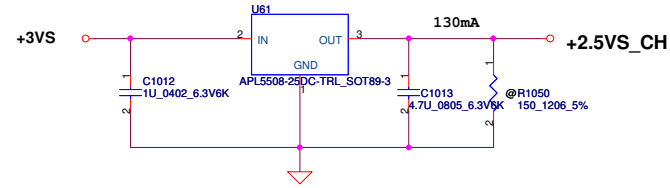
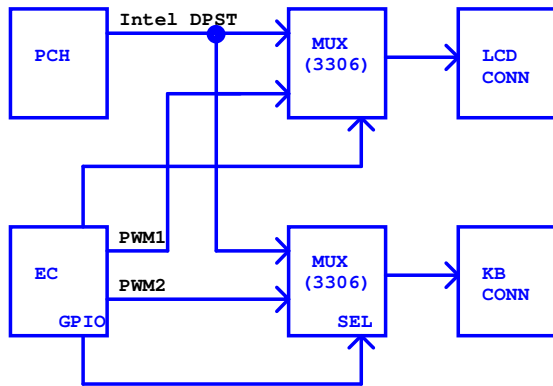
4/1 add for RF



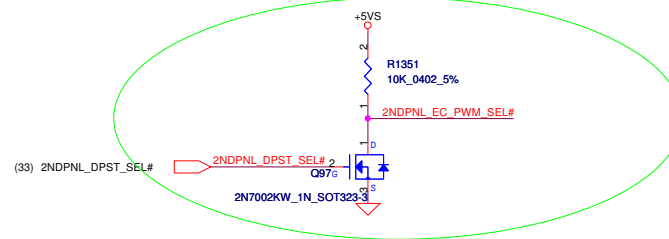
Add R1350 3/18 DISP
Move R154 From PCH side to JLVDS side 3/18

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Issued Date	2009/11/23	Deciphered Date	2010/11/23	Title	
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				Size	Rev
				Custom	0.1
Date: Monday, November 22, 2010				I\Sheet 22 of 51	
PAU30 M/B LA-6392P Schematic					

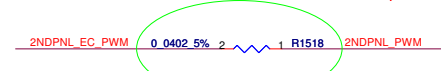
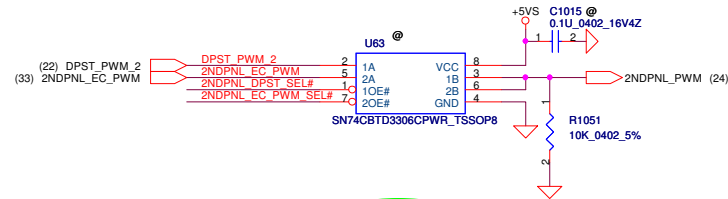
Brightness control



Change 2NDPNL_DPST_SEL# Circuit 3/18



change U63,C1015 BOM structure from pop to @ 08/25



Add R1518 08/24

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								Size	Document Number	Rev
								Customer	PAU30 M/B LA-6392P Schematic	1.0
Date:		Monday, November 22, 2010		Sheet		23		of 51		

CRT Connector

Change L30,L32,L34 from SM01000HJ00 to SHI0000A800 11/01

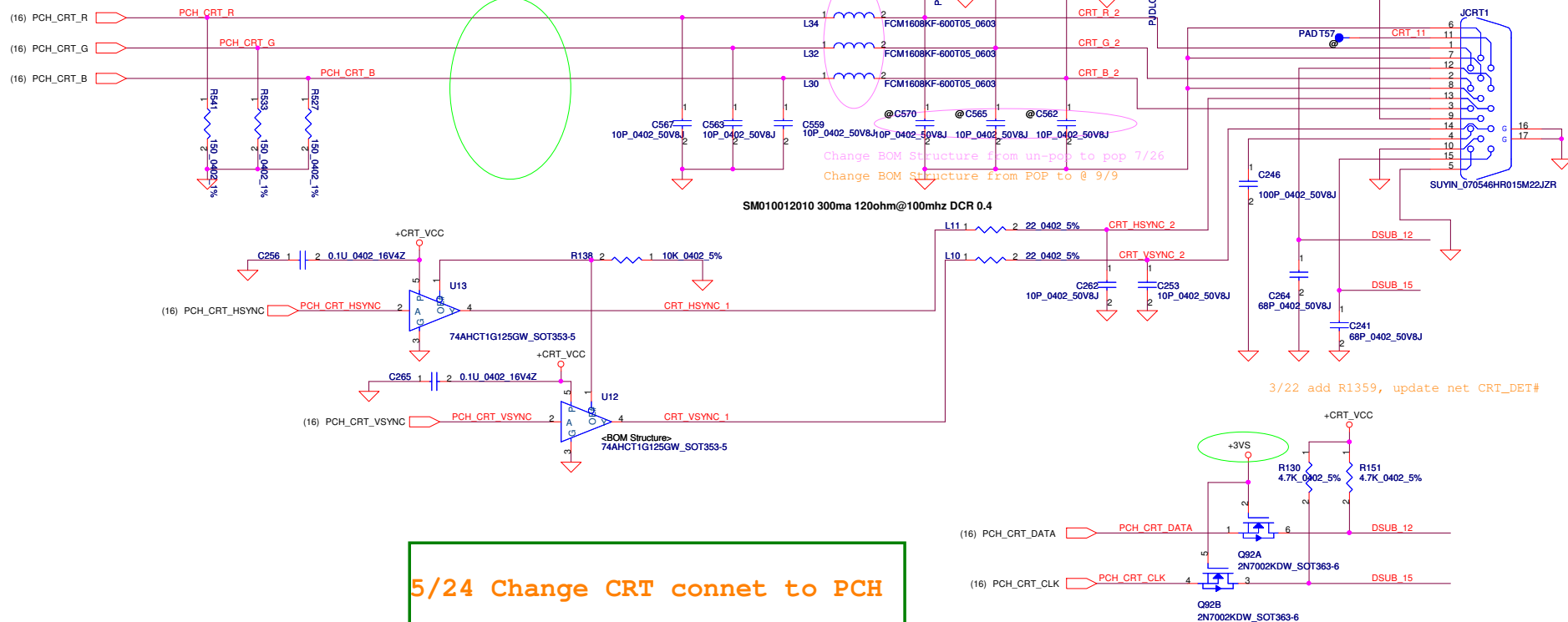
Change L30,L32,L34 P/N form SM01000HI00 to SM01000HJ00 (bead 60 ohm) 9/9

Del L77.L78.L79.C571.C564.C561 3/4
NV DG RGB recommended one pi filter

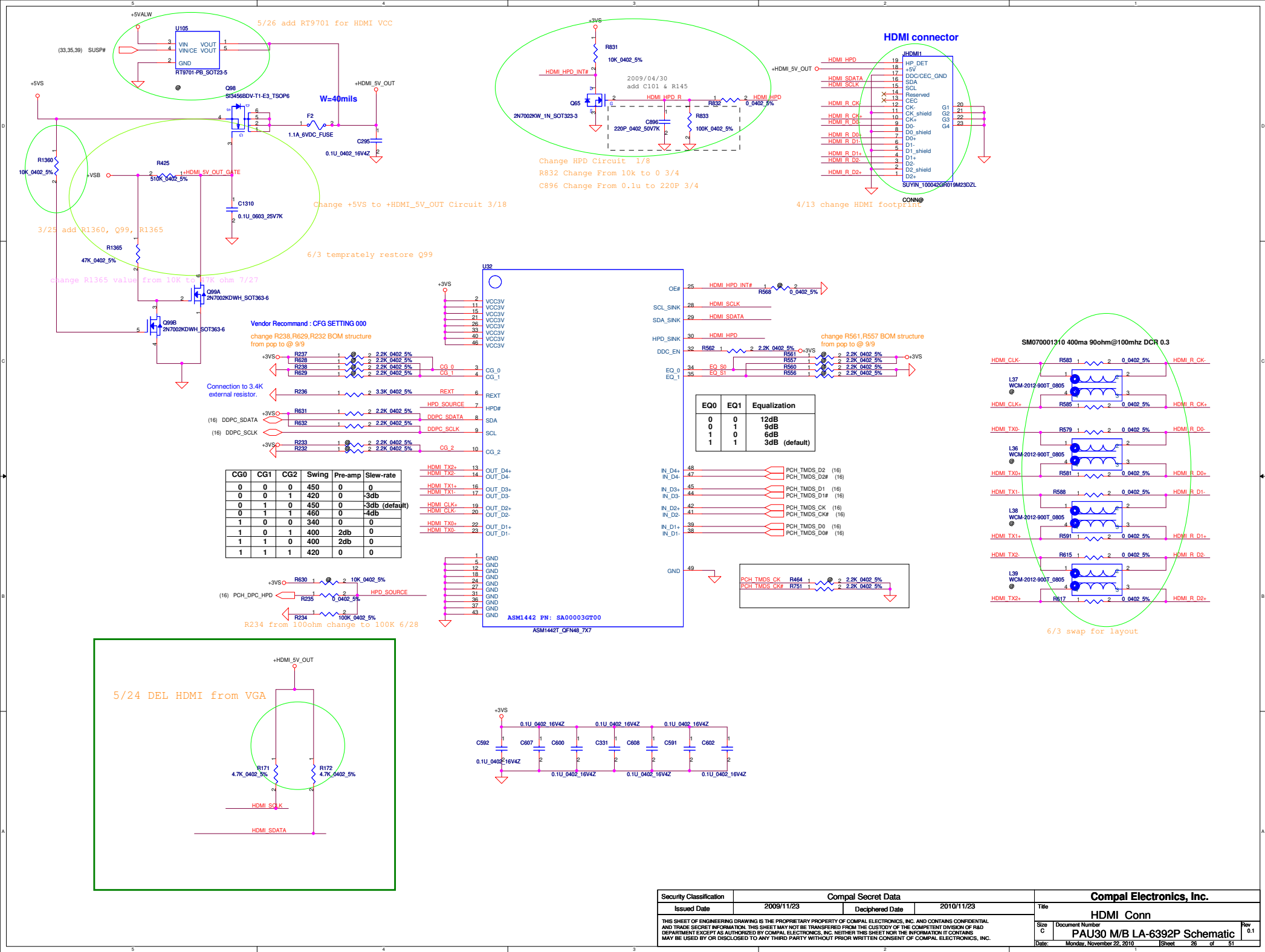
Change from Inductor to Bead 60 ohm 7/26

Change ESD protect circuit (follow NAV50) 3/12
Close to CRT CONN for ESD.

5/26 change to fuse

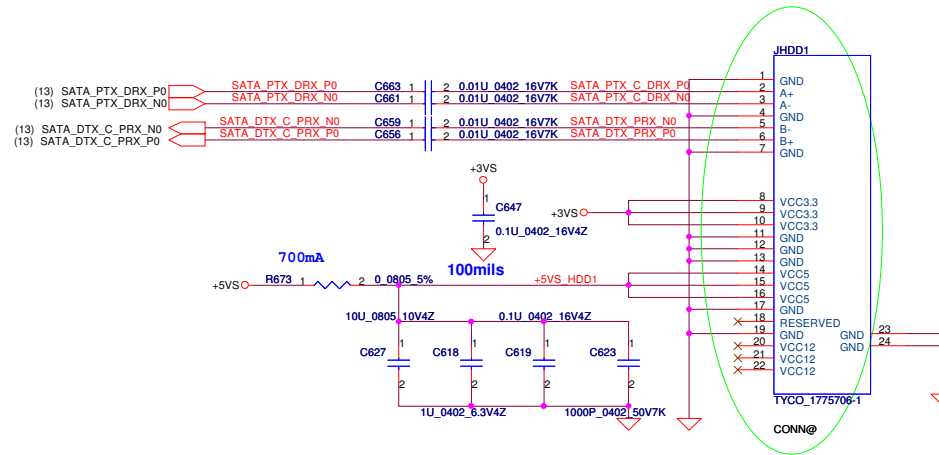


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2009/11/23				2010/11/23				CRT Connector			
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Size B				Document Number				Rev 0.1			
PAU30 M/B LA-6392P Schematic											



CL 4.0 mm

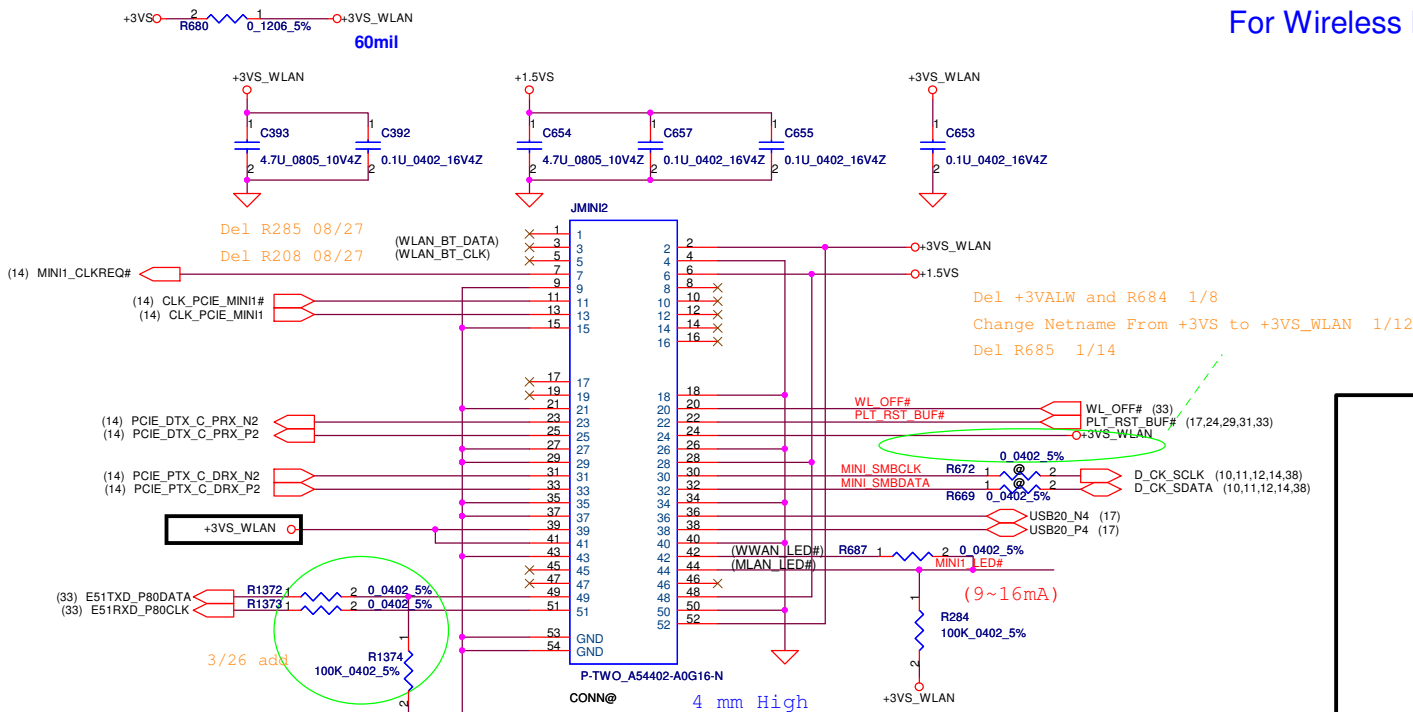
SATA HDD1 Conn.



6/8 change HDD symbol
change HDD symbol 8/26

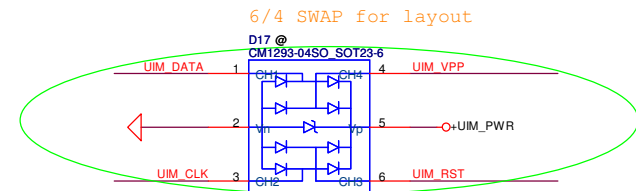
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/11/23	Deciphered Date	2010/11/23	Title HDD & ODD Connector	
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				Date: Monday, November 22, 2010	Sheet 27 of 51

For Wireless LAN (Half Card)



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

For SIMM CARD

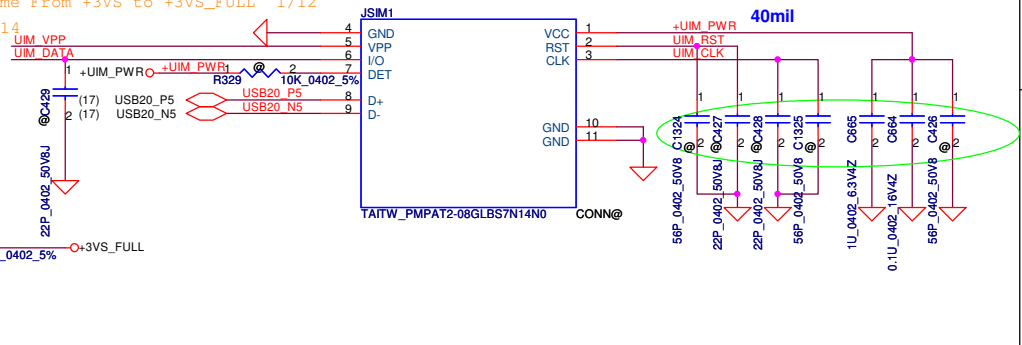
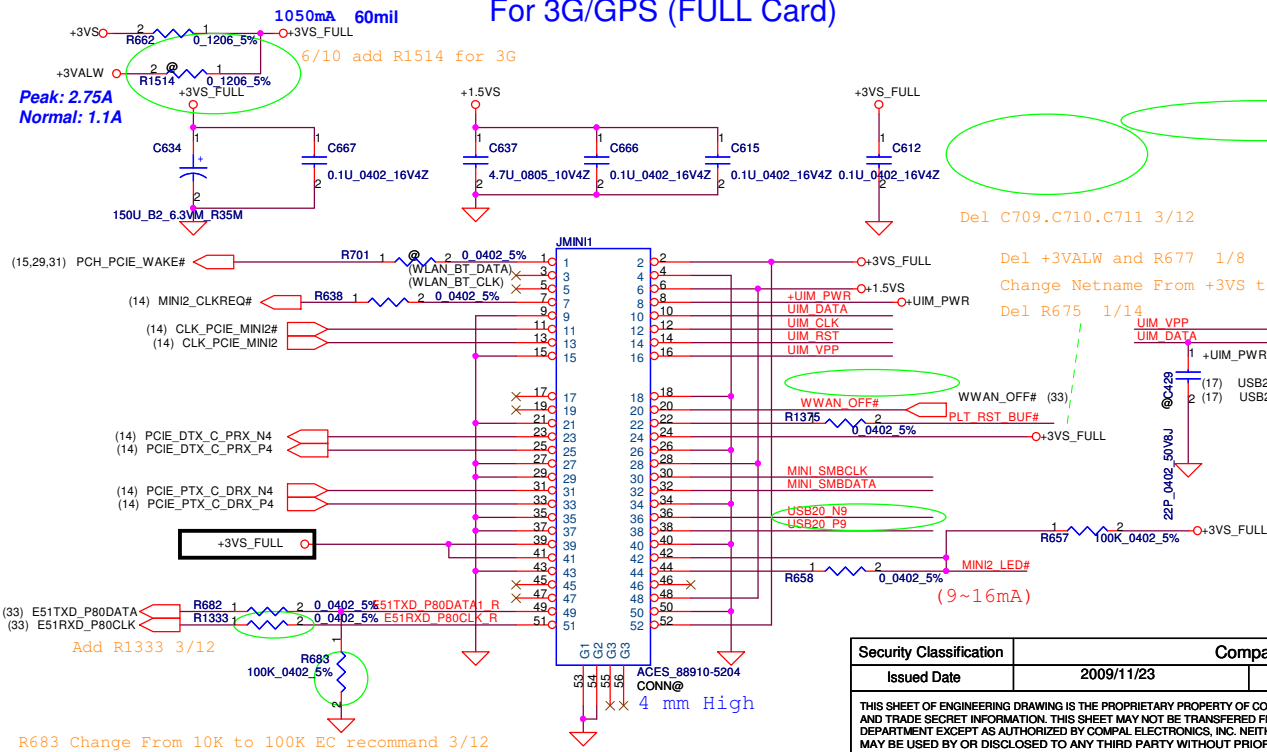


Del L41.R661.R663 1/14

Change Netname From USB20_N10_1 to USB20_N10 1/12

Change Netname From USB20_P10_1 to USB20_P10 1/12

For 3G/GPS (FULL Card)

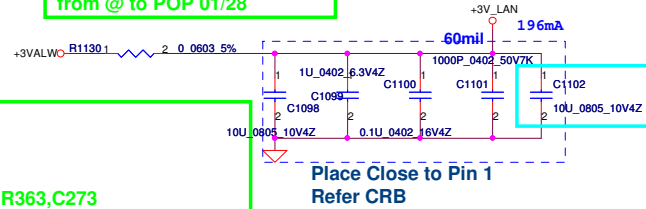


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				Customer	PAU30 M/B LA-6392P Schematic	
Date:				Monday, November 22, 2010	Sheet 28 of 51	

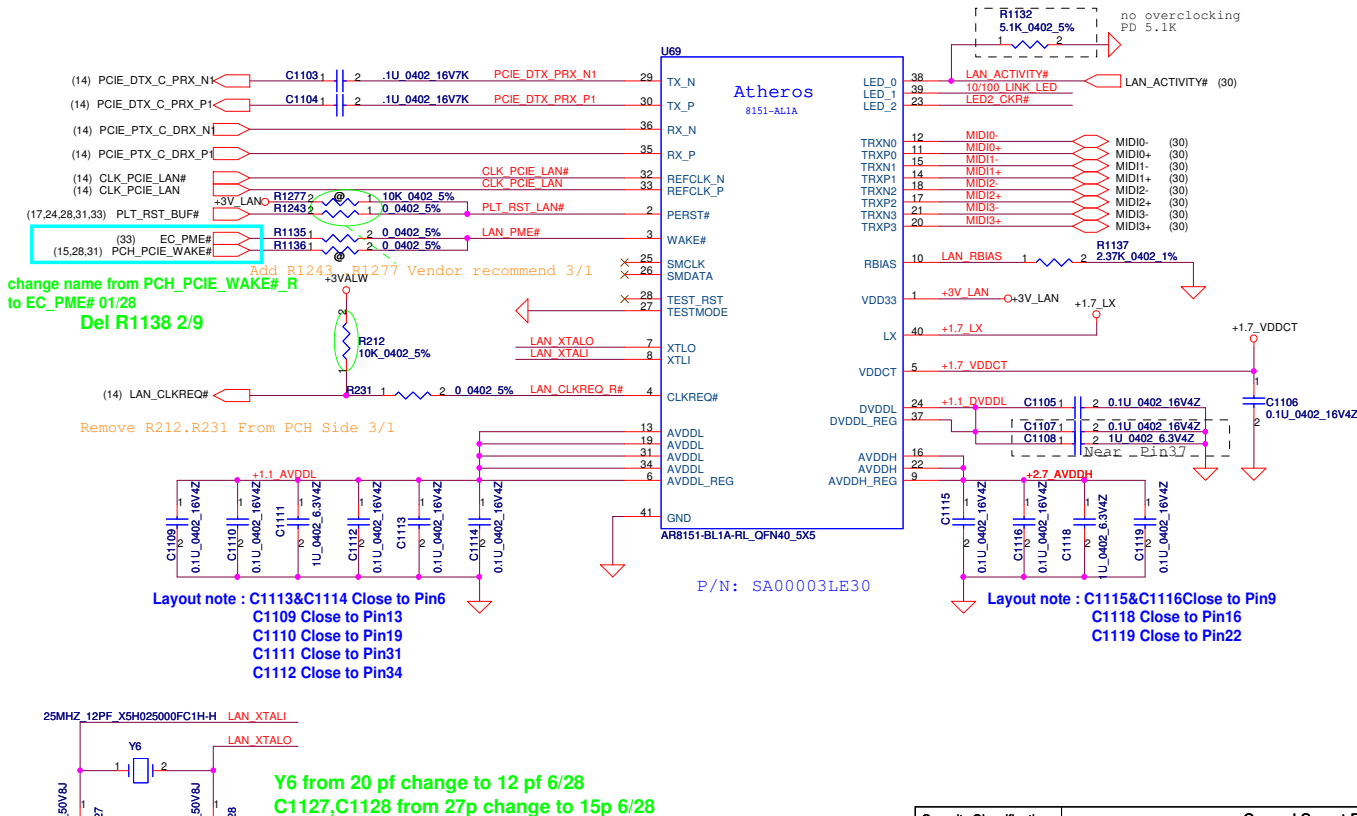
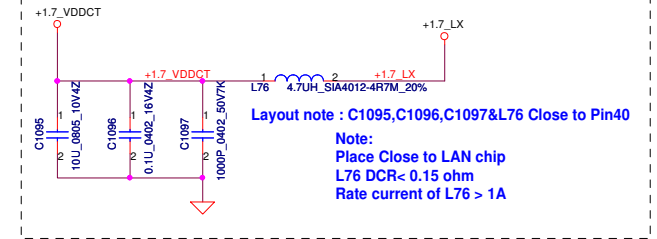
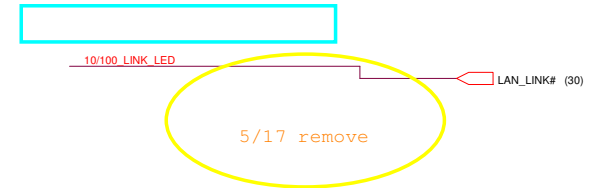
LAN Power Circuit & Refer NTUC0

change R362 BOM structure
from @ to POP 01/28

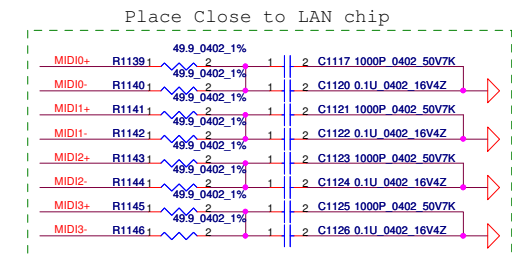
Del Q21,R363,C273
(WOL function) 01/28



10/22 Remove R364



10/22 Change R376 from mount to @
11/02 Change R373 from mount to @
11/02 Delete Q3(@),R375(@),R377(@)
11/09 Delete R373(@),R376(@)



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Size	Custom	Document Number	PAU30 M/B LA-6392P Schematic	Rev	0.3
Date	Monday, November 22, 2010	Sheet	29	of	51

Copy NIMUA

change transformer P/N from TAIMAG(SP050004M00)
change to BOTHHAND (SP050006B00) 9/9
BOTHHAND (SP050006B00)

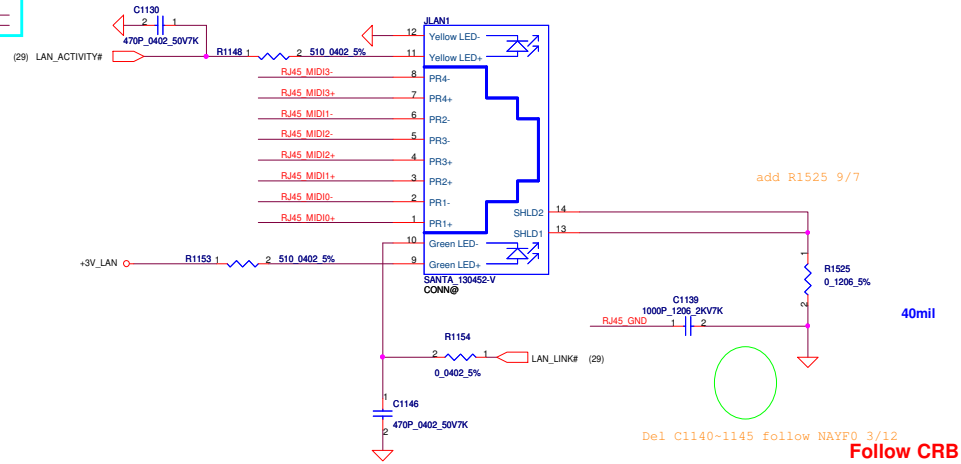
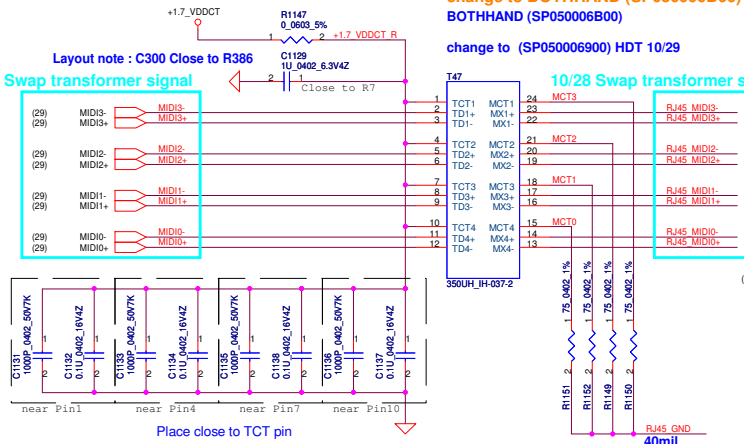
change to (SP050006900) HDT 10/29

Layout note : C300 Clos

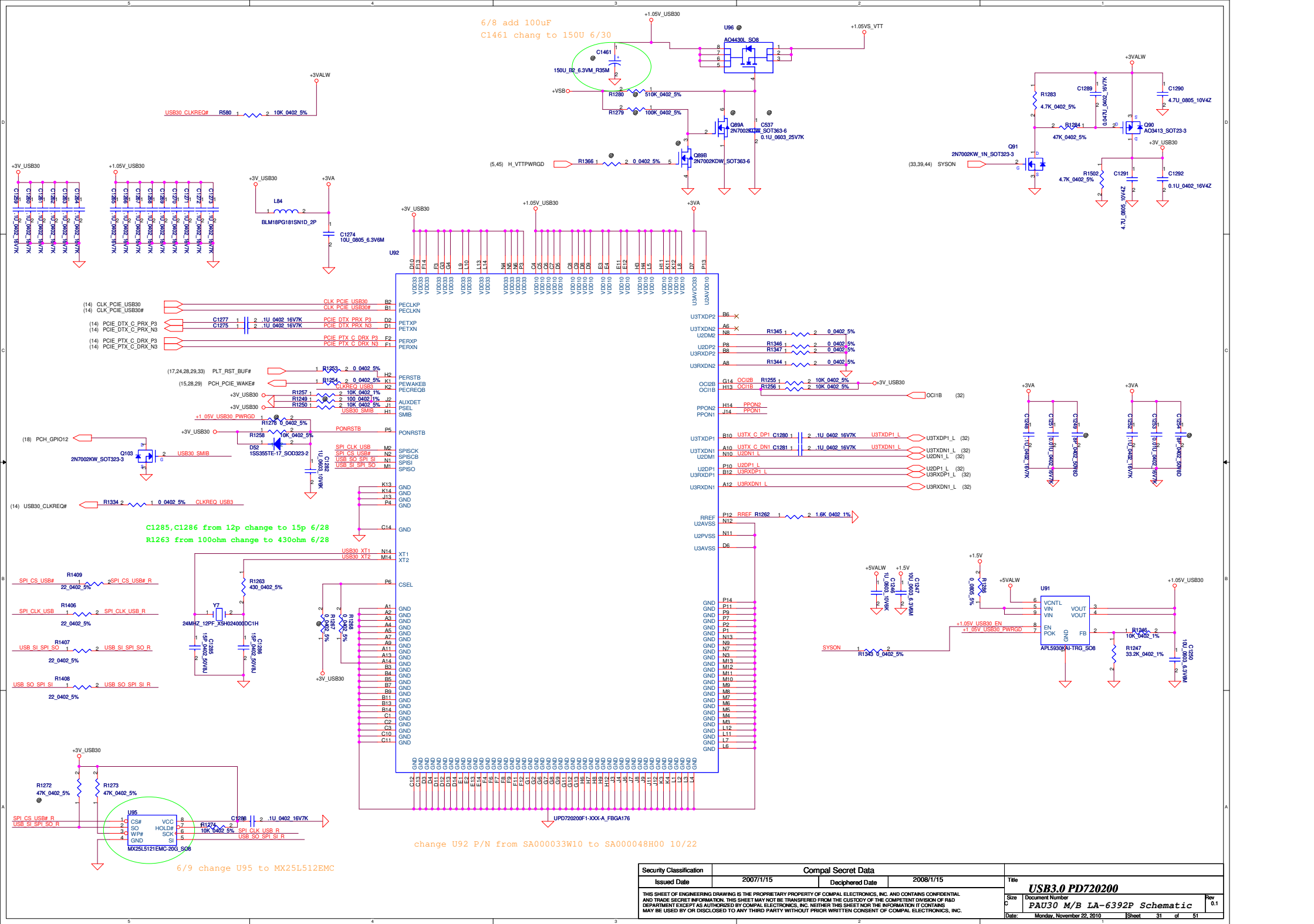
10/28 Swap transformer signal

Layout note : C300 Close to R386

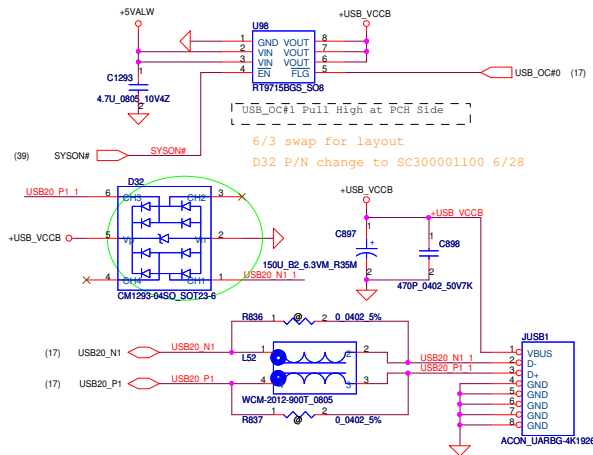
10/28 Swap transformer signal



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					PAU30 M/B LA-6392P Schematic	0.3
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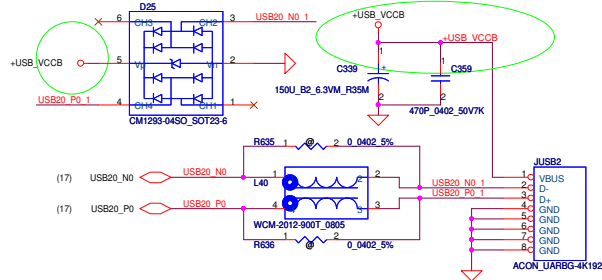


Left

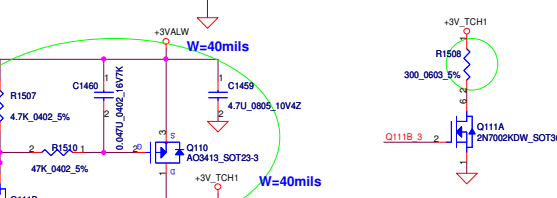
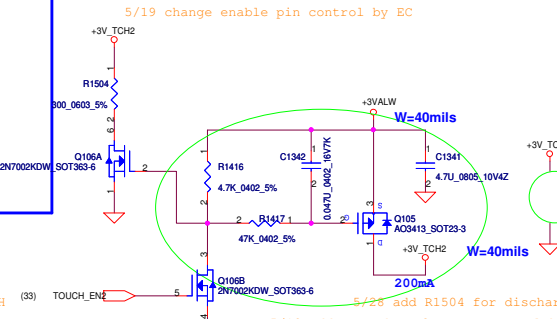
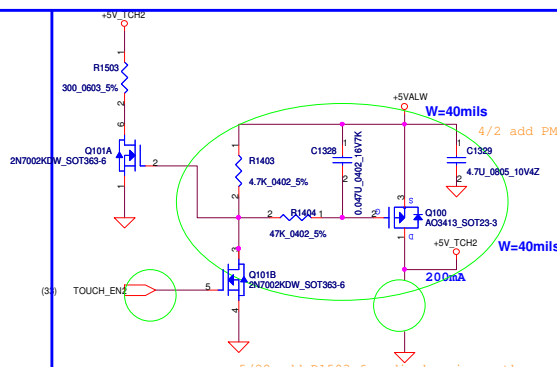
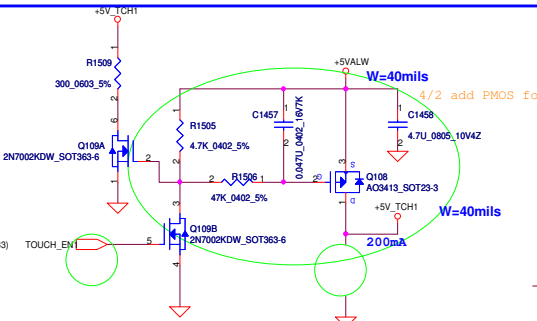
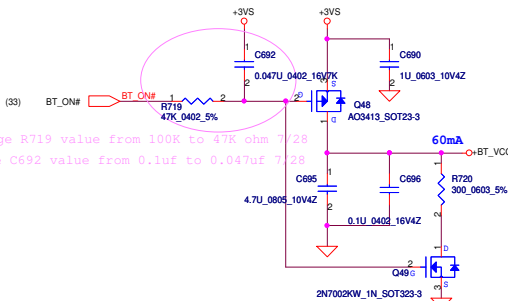
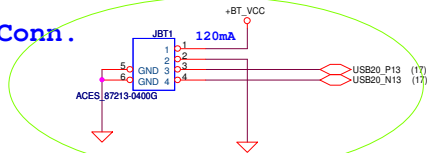


3/22 Change JUSB2 power net

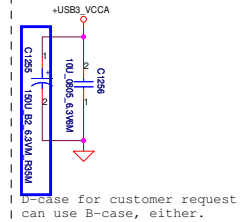
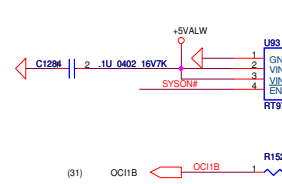
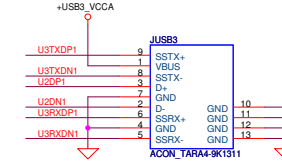
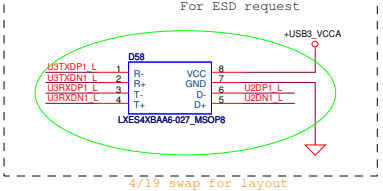
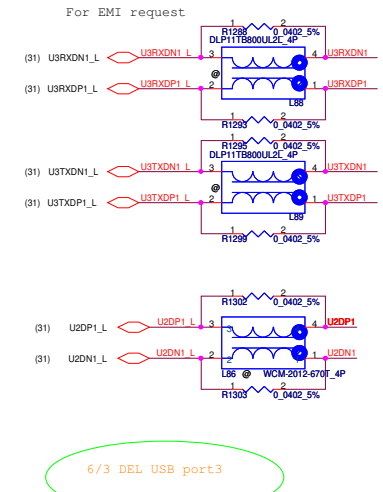
D25 P/N change to SC300001100 6/28



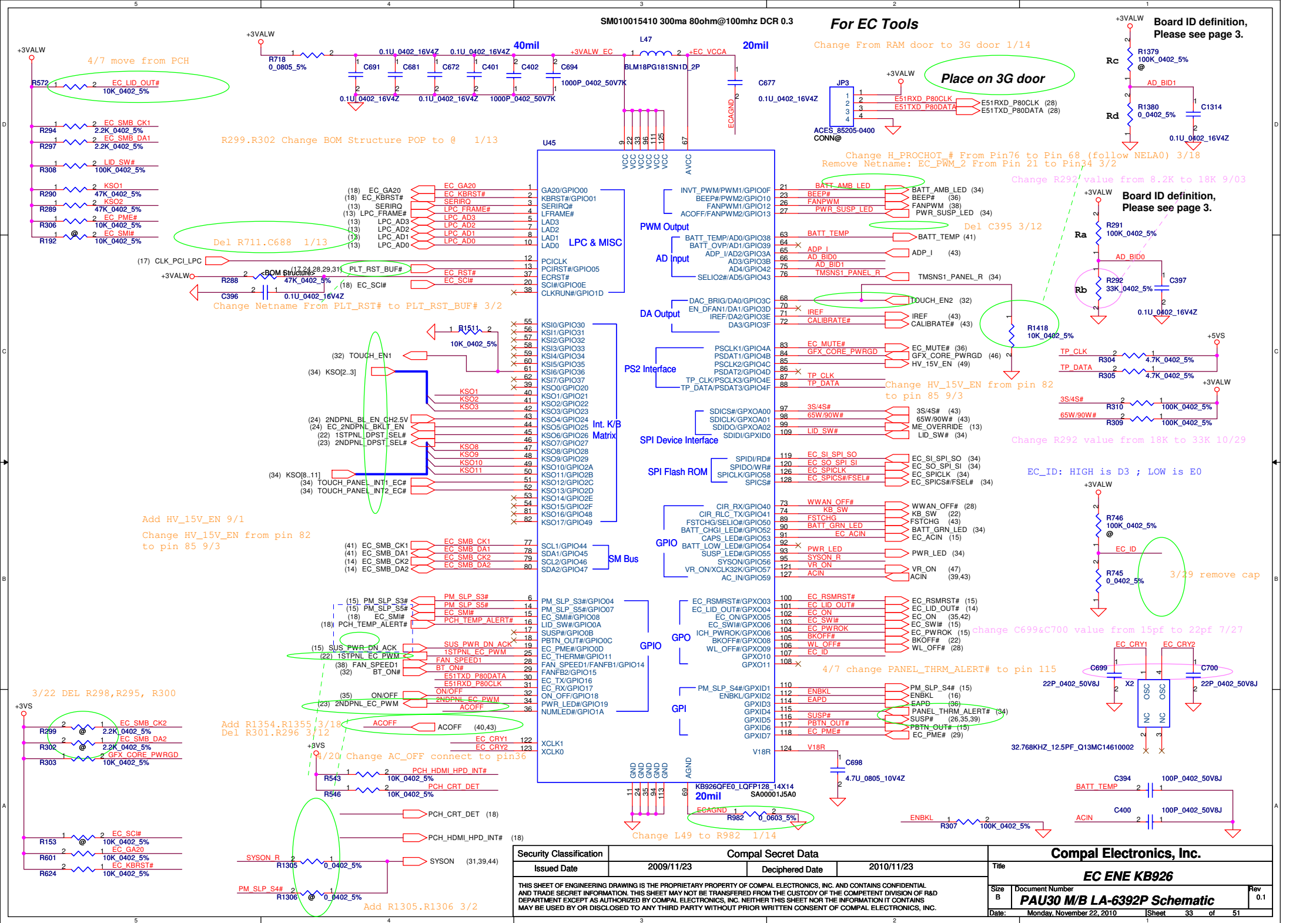
BT Conn.

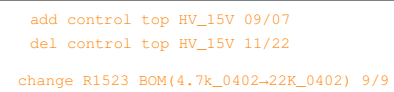


Right



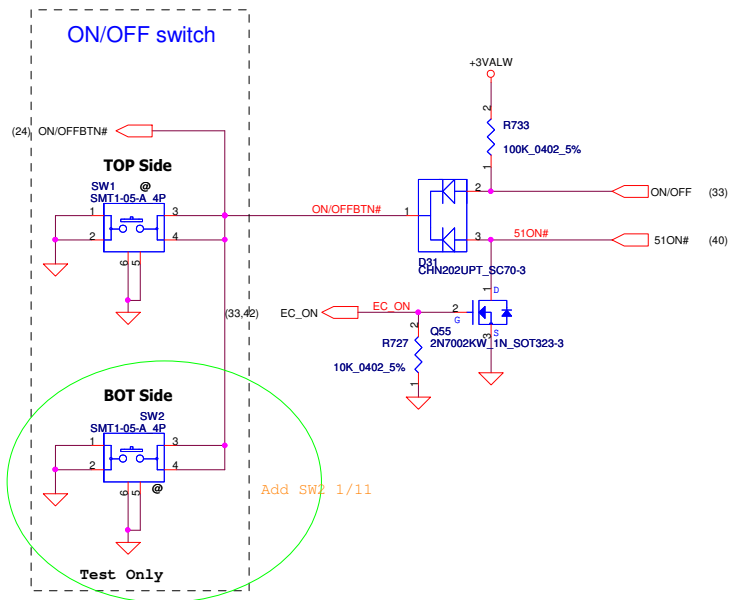
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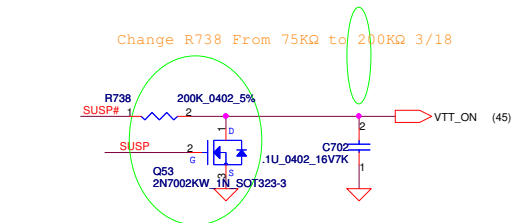
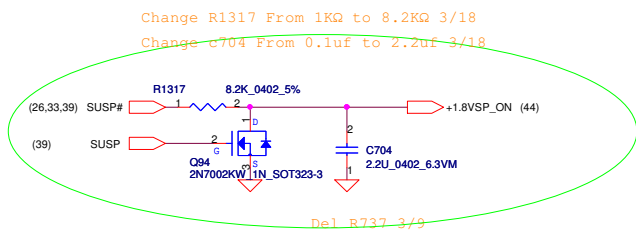


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				Document Number PAU30 M/B LA-6392P Schematic	0.1
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Power Button

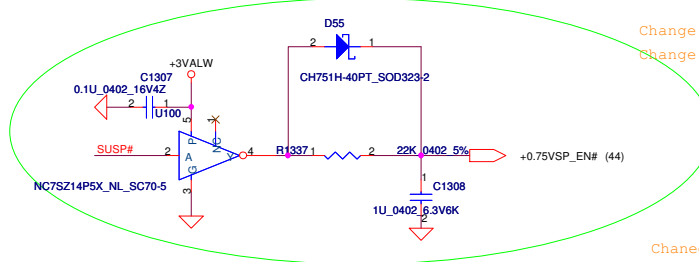


Power ON Circuit



Add +0.75VSP_EN Circuit 3/13

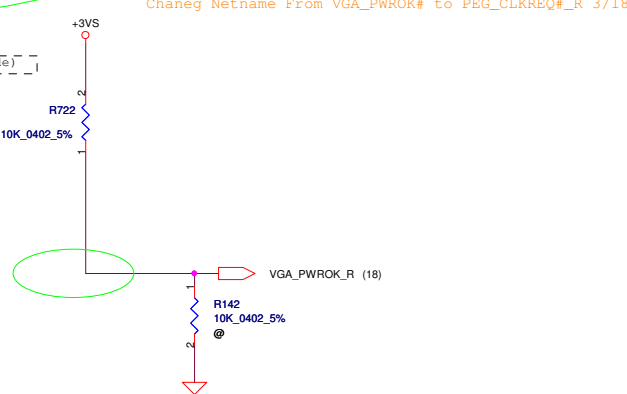
Change +3VS to +3VALW 3/16



Change C1308 From 0.1uF to 1uF 3/18

Change R1337 From 1KΩ to 22KΩ 3/18

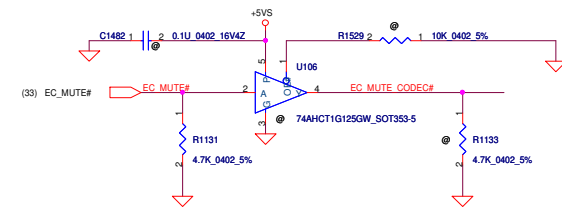
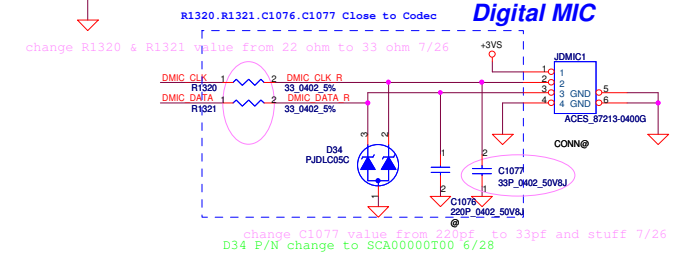
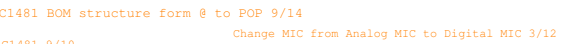
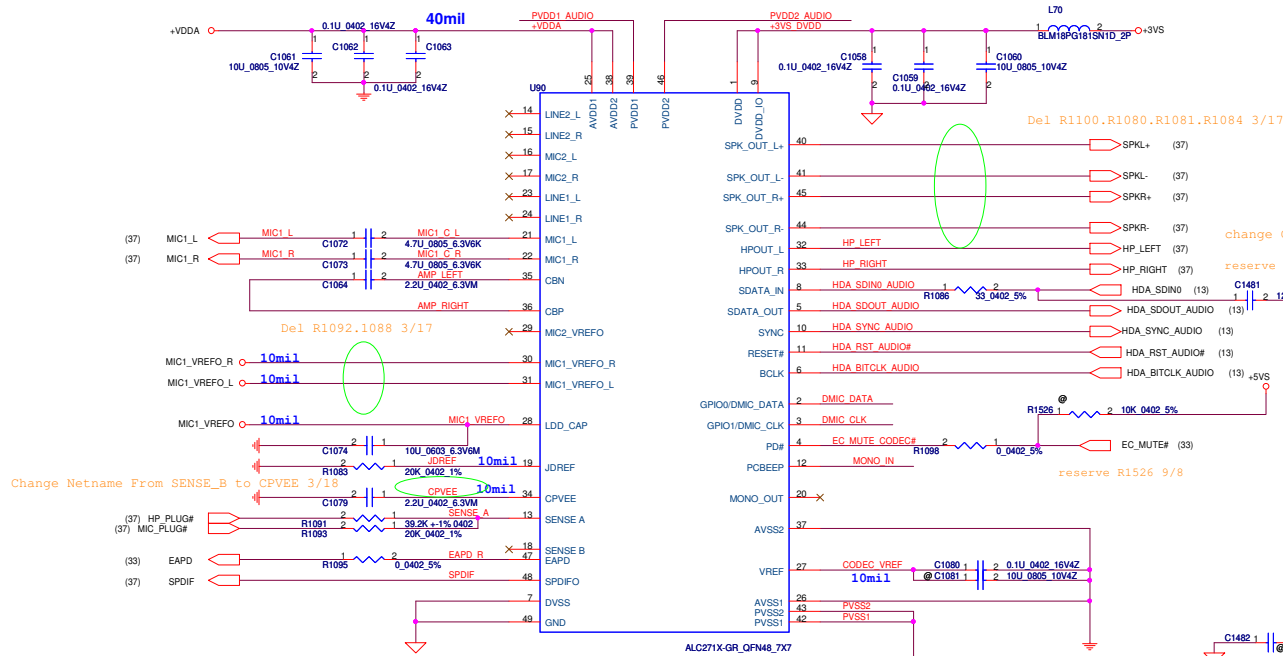
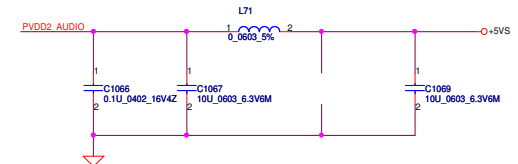
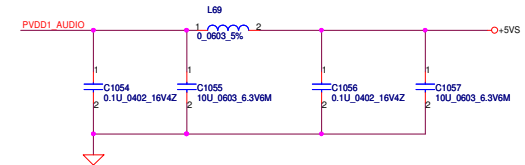
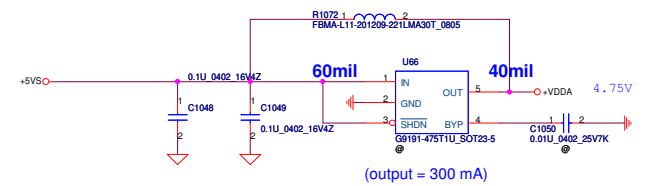
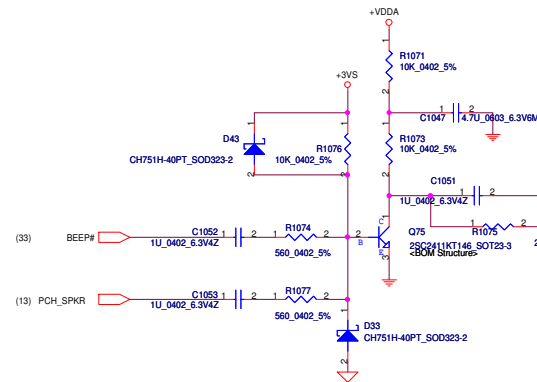
[VGA_PWROK is Open-Drain (Pull high at HW'side)]



Del U46,R734,R1159,R739,R740,D45,R729,R730,D46 3/9

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				PAU30 M/B LA-6392P Schematic	
				Date	Monday, November 22, 2010
				Sheet	35 of 51
				Rev	0.1

Del ALC272 circuit 3/12

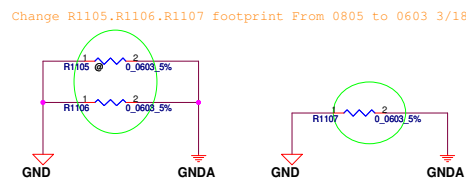


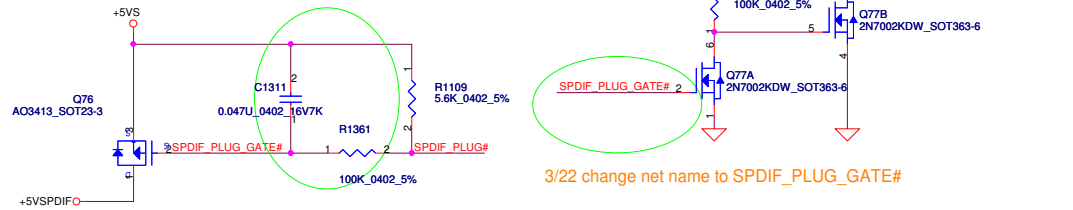
Reserve C1428,U106,R1529,R1133 10/22

Add R1131 10/22

Need update this table

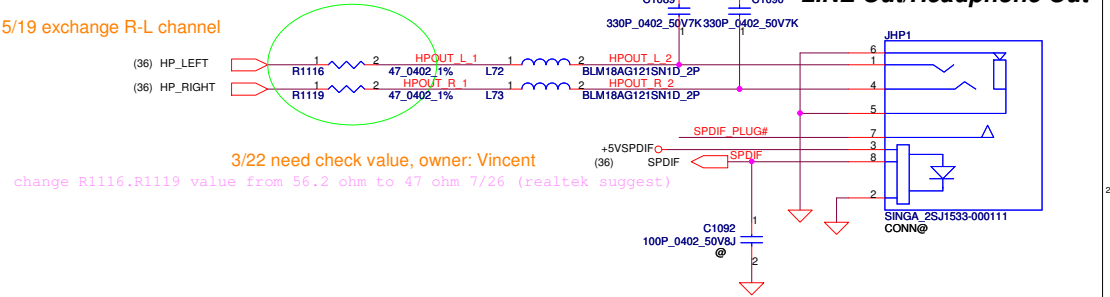
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



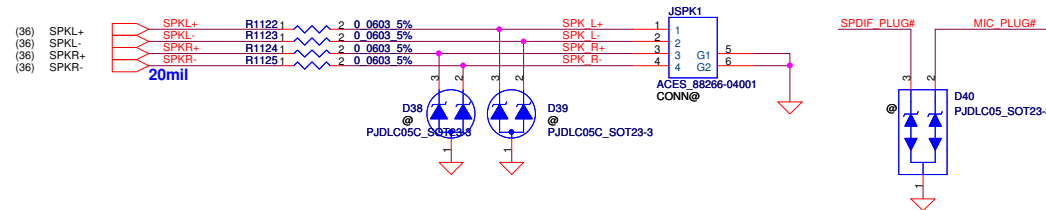


20mil
change back R1361 value from 56k ohm to 100K ohm 7/26
change C1311 value from 0.1u to 0.047uf 7/28

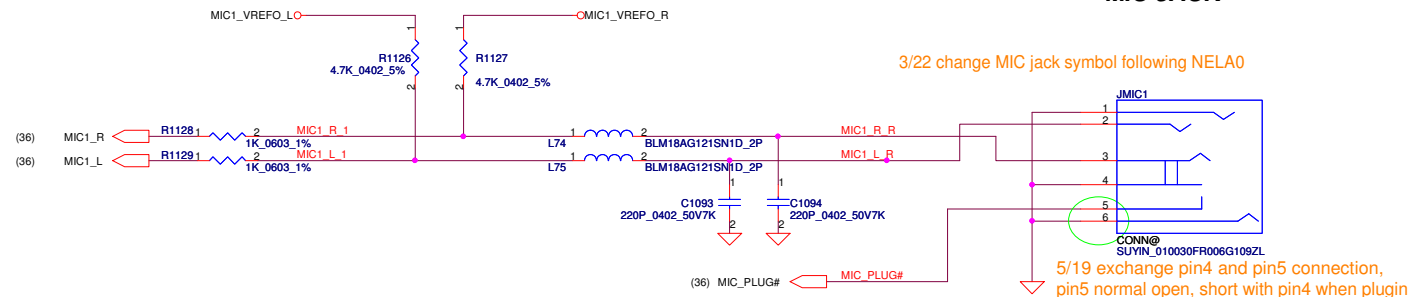
5/19 exchange R-L channel



Int. Speaker Conn.

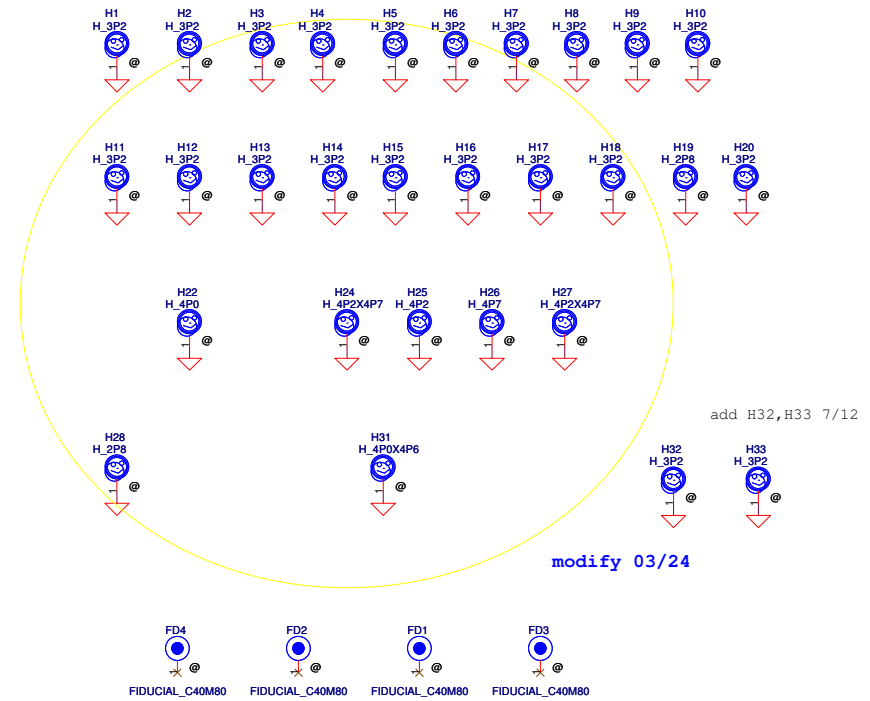
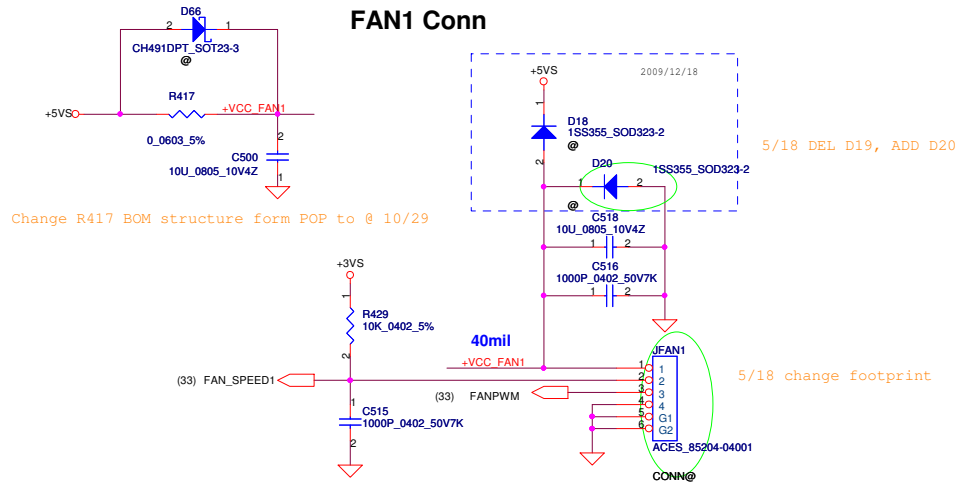


MIC JACK



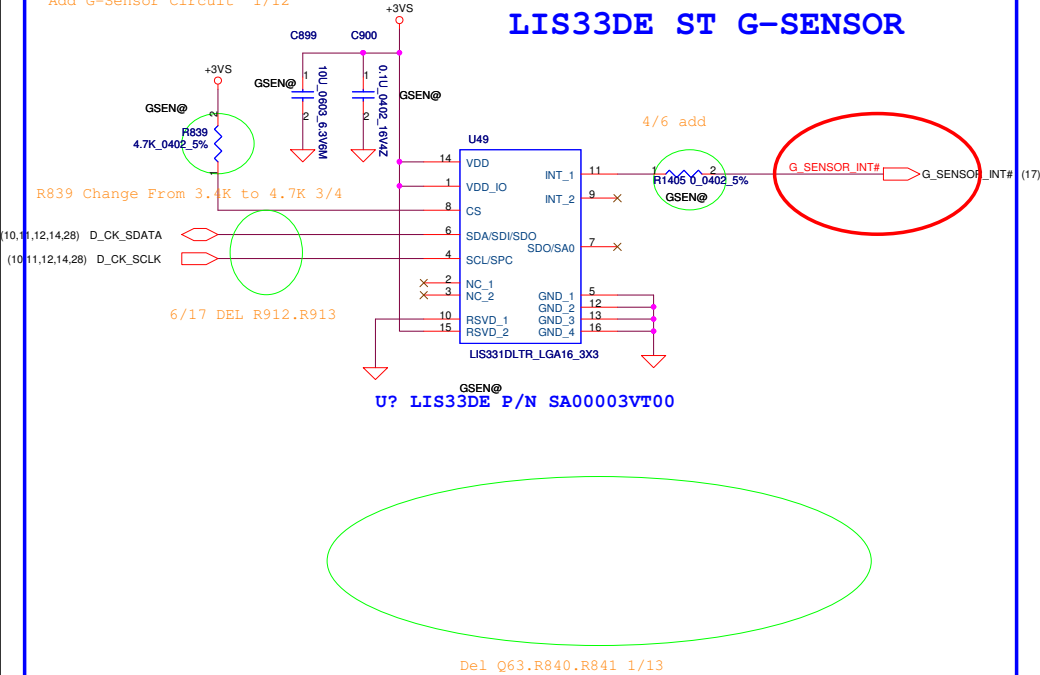
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				PAU30 M/B LA-6392P Schematic	
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Change D66 BOM structure form @ to POP 10/29
reserve D66 10/26

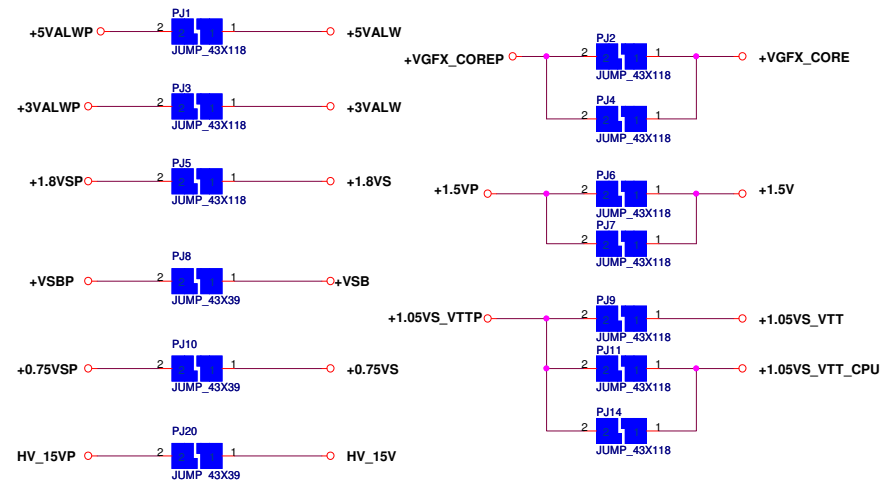
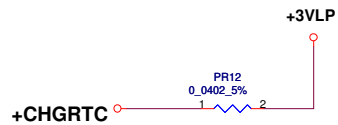
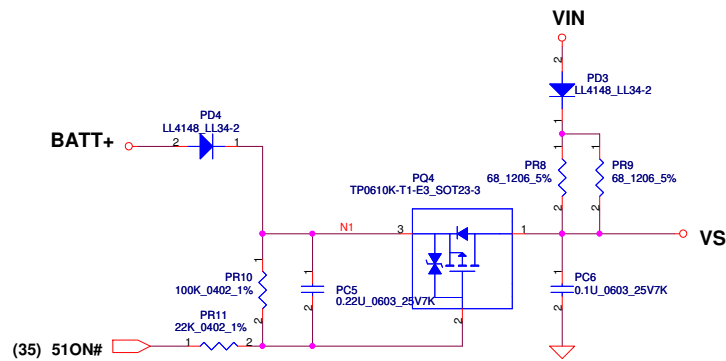
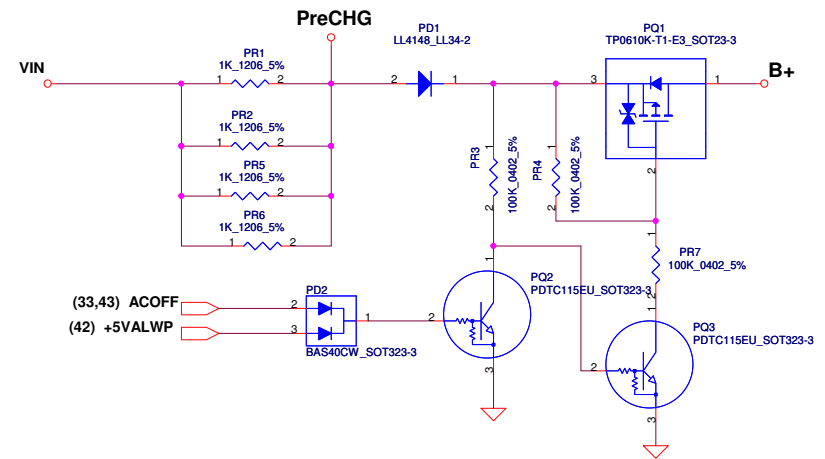
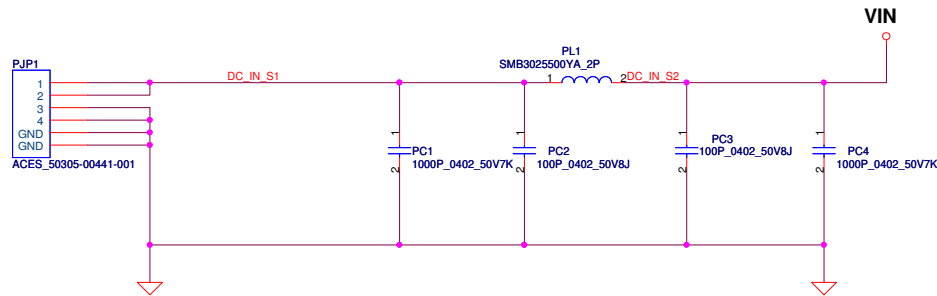


Add G-Sensor Circuit 1/12

LIS33DE ST G-SENSOR

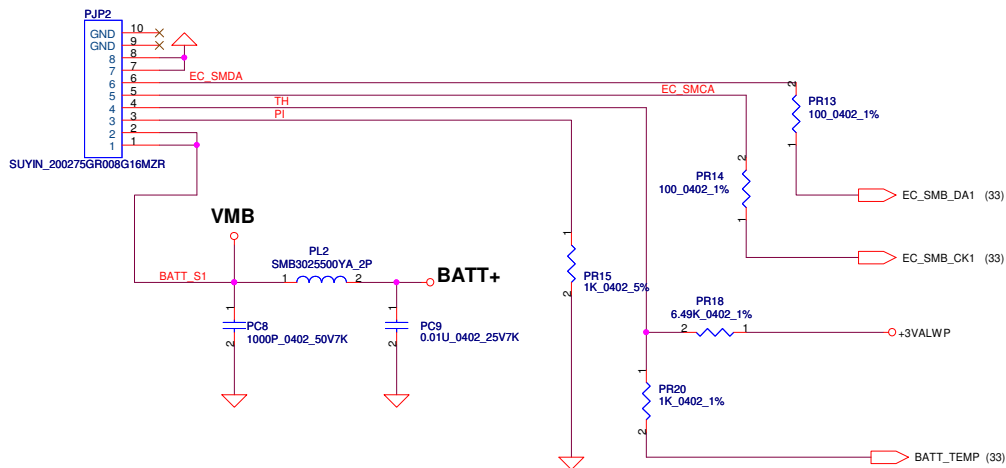


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						Size B	Document Number			Rev 0.1	
						PAU30 M/B LA-6392P Schematic					
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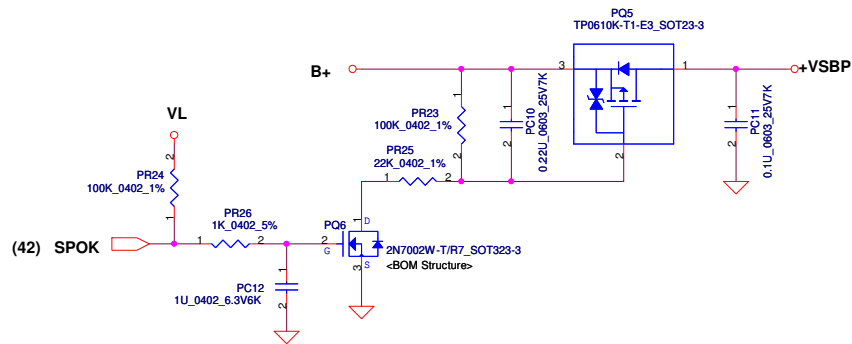
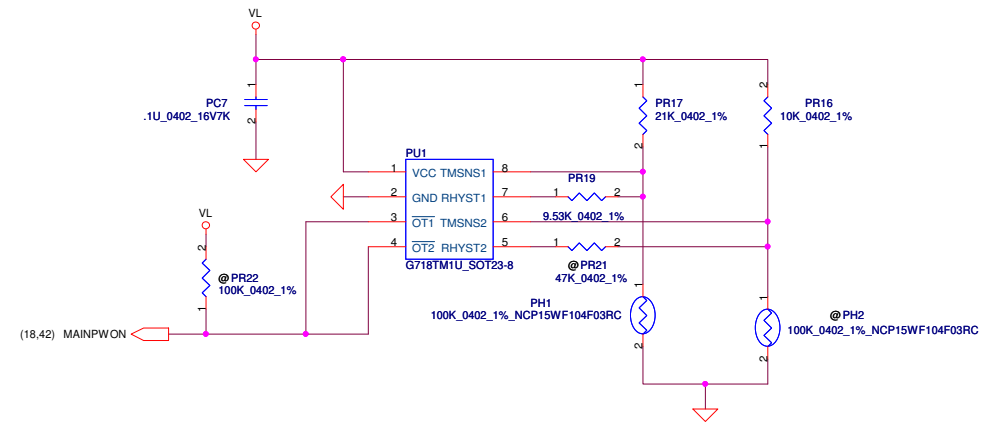
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Issued Date				2009/11/23		Deciphered Date		2010/11/23		Title	
										DCIN & PRECHARGE	
										SR40 Schematic	
										Rev 0.1	
										Date: Monday, November 22, 2010	
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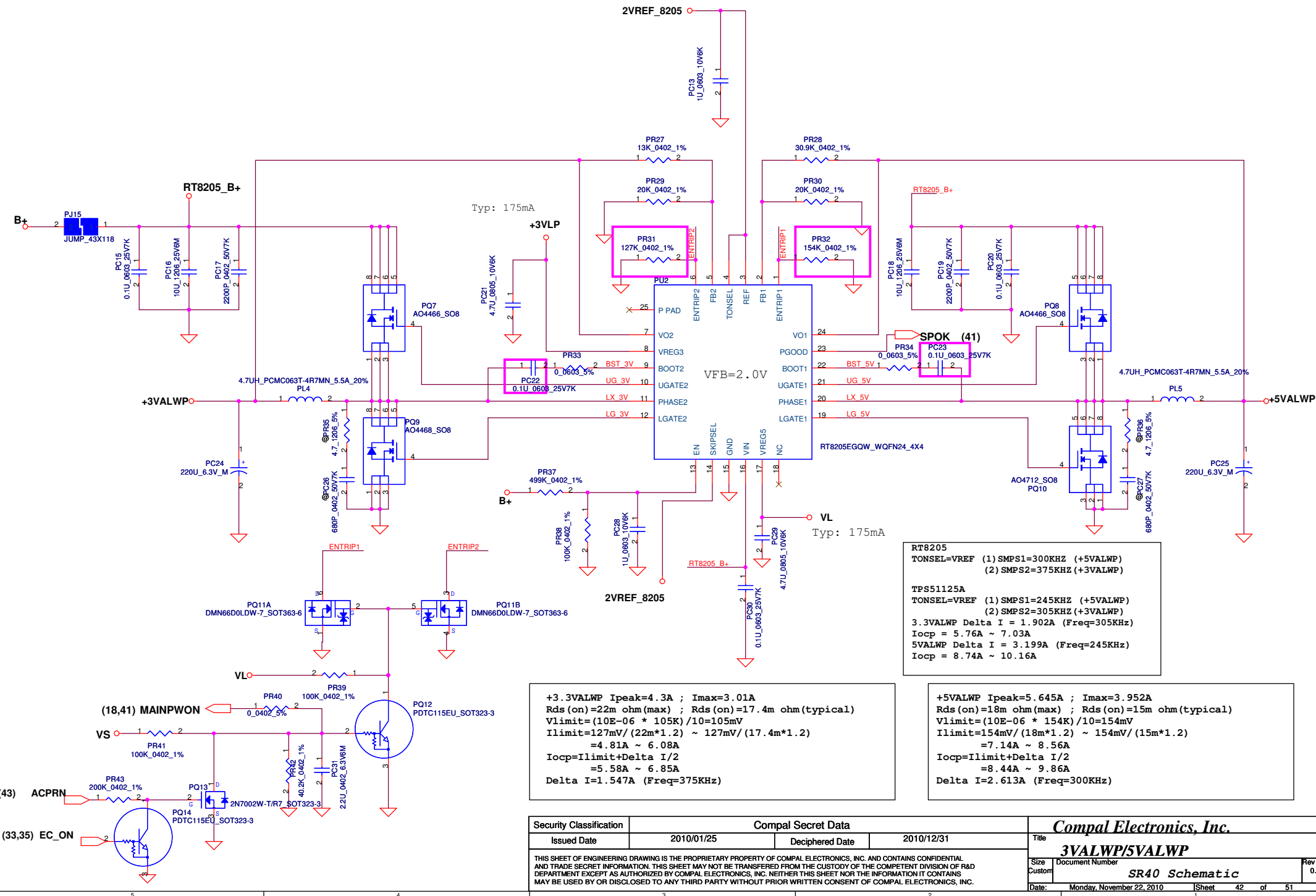
PH1 under CPU botten side :

CPU thermal protection at 92 degree C
Recovery at 56 degree C



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				BATTERY CONN / OTP	
				Size	
Custom		Document Number		Rev	
		SR40 Schematic		0.1	
Date:		Monday, November 22, 2010		Sheet 41 of 51	

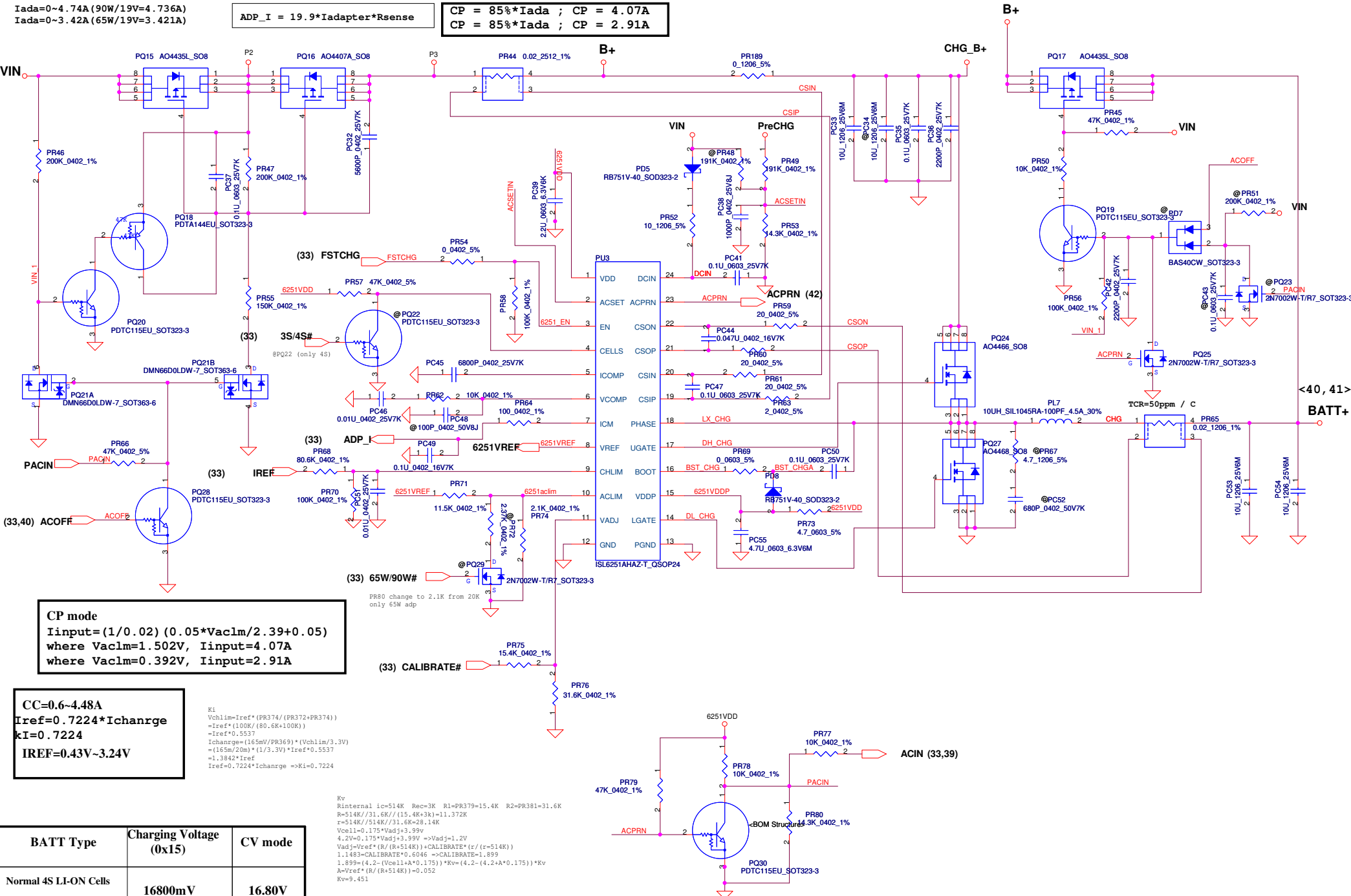
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



I_{ada}=0~4.74A (90W/19V=4.736A)
I_{ada}=0~3.42A (65W/19V=3.421A)

ADP_I = 19.9*I_{adapter}*R_{sense}

CP = 85%*I_{ada} ; CP = 4.07A
CP = 85%*I_{ada} ; CP = 2.91A



CP mode
I_{input}=(1/0.02) (0.05*V_{ac1m}/2.39+0.05)
where V_{ac1m}=1.502V, I_{input}=4.07A
where V_{ac1m}=0.392V, I_{input}=2.91A

CC=0.6~4.48A
I_{ref}=0.7224*I_{charge}
kI=0.7224
I_{REF}=0.43V~3.24V

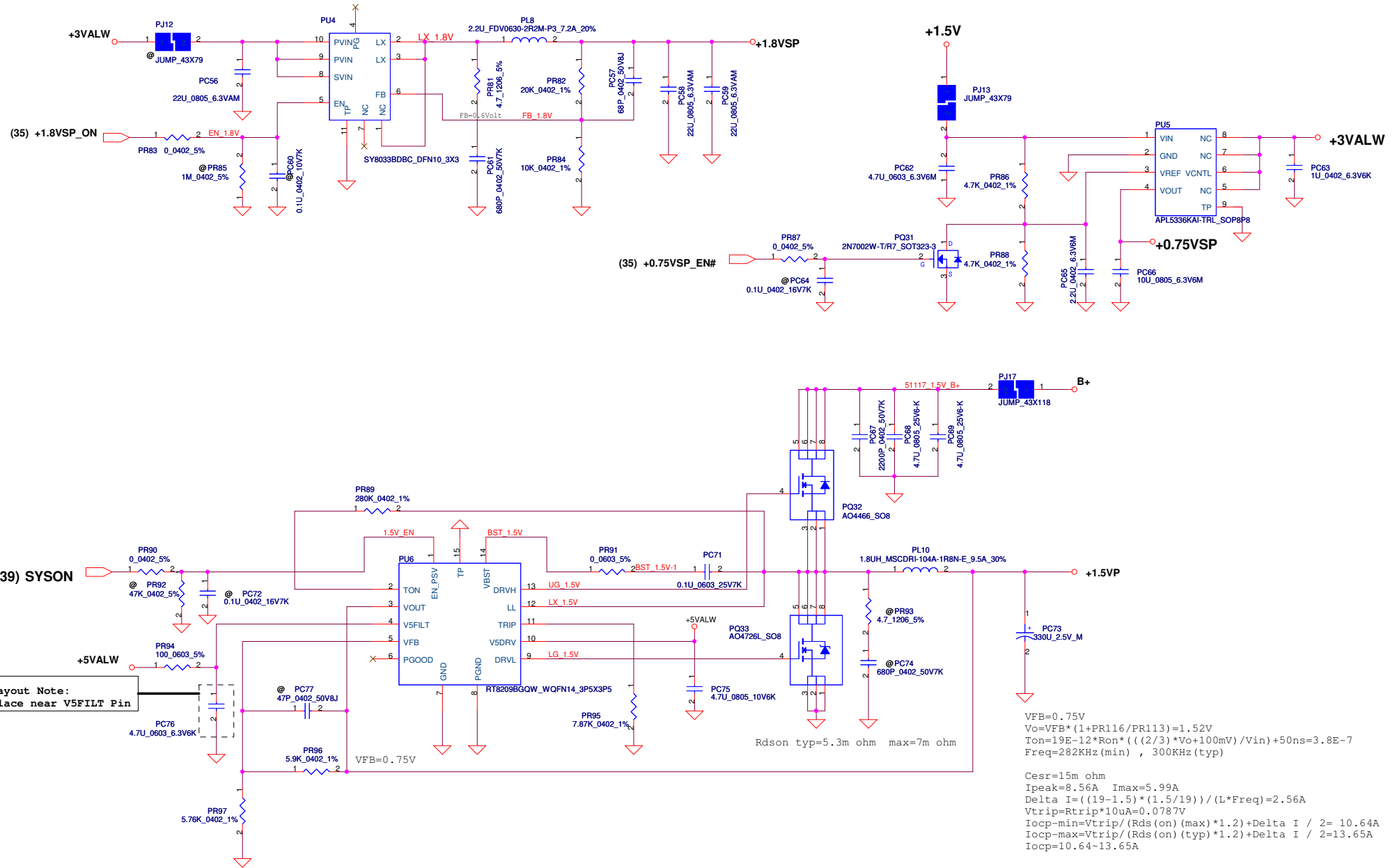
K1
V_{chlim}=I_{ref}*(PR374/(PR372+PR374))
=I_{ref}*(100K/(80.6K+100K))
=I_{ref}*0.5537
I_{charge}=(165mV/PR369)*(V_{chlim}/3.3V)
=(165mV/20m)*(1/3.3V)*I_{ref}*0.5537
=1.3842*I_{ref}
I_{ref}=0.7224*I_{charge} =>K1=0.7224

Kv
R_{internal} ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
R=514K/(514K/(15.4K+3K))+11.372K
r=514K/(514K/(31.6K+28.14K))
V_{oc11}=0.175*V_{adj}+3.99V
4.2V=0.175*V_{adj}+3.99V =>V_{adj}=1.2V
V_{adj}=V_{ref}*(R/(R+514K))+CALIBRATE*(r/(r+514K))
1.1485=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(V_{oc11}+0.175))*Kv=(4.2-(4.2+0.175))*Kv
A=V_{ref}*(R/(R+514K))=0.052
Kv=9.451

BATT Type	Charging Voltage (0x15)	CV mode
Normal 4S LI-ON Cells	16800mV	16.80V

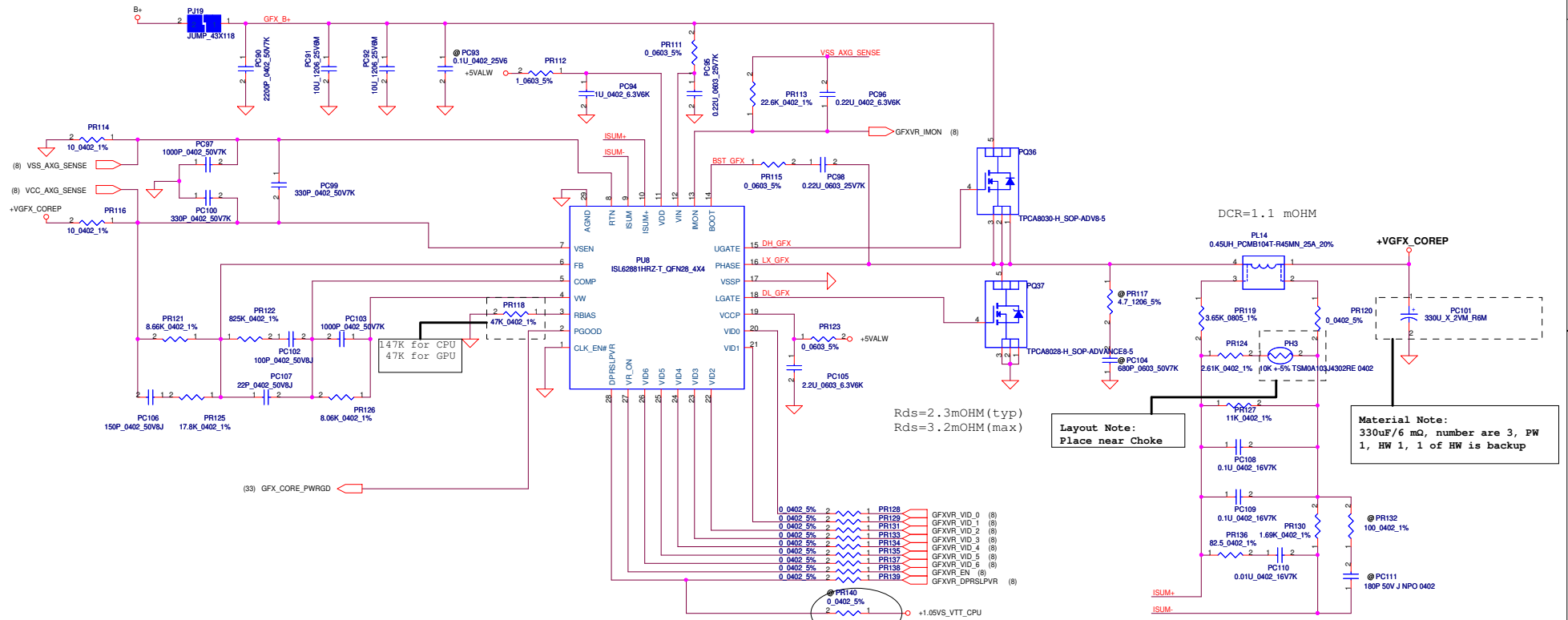
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				Document Number	SR40 Schematic
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				Rev	0.1

Note:Iload(max)=3.5A



Intel Auburndale CPU(Integrate Graphics) Ipeak=22A Imax=15A
 OCP calculation : Assume DCR=1.1m ohm
 $G1 = R_n / (R_n + R_{sum}) = 0.617$
 where $R_n = PR127 // (PR124 + PH3) = 5.875k \text{ ohm}$
 $R_{sum} = PR119 = 3.65k \text{ ohm}$
 $LL = 2 * R_{droop} * G1 * DCR / R_i = 6.96m \text{ V/A}$
 where $R_{droop} = PR121 = 2.87k \text{ ohm}$, $R_i = PR130 = 562 \text{ ohm}$
 $I_{ocp} = OCP \text{ Threshold} * R_{droop} / LL = 24.89A$

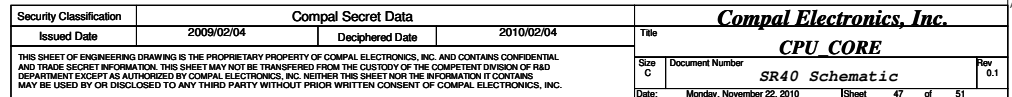
Vvid = 1.25
 LL = 7m ohm
 Iccaxg = 22A
 $I_{cctdc_axg} = 12 \text{ A}$
 Iccaxg_dyn 19 A



2009-1214 common circuit modify.

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2009/4/15		2010/04/15		GFX COREP	
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	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD

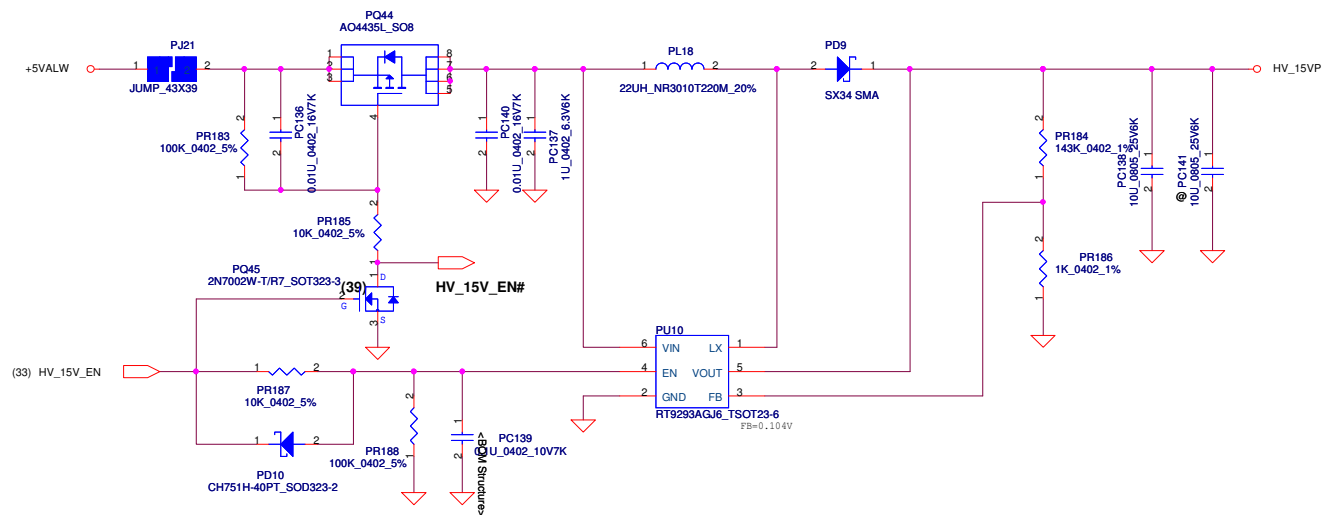


Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	change bead to jump	6 layers change to 8 layers, so change bead to jump	0.1	50	1 del PC14 SE074681K80 (S CER CAP 680P 50V K X7R 0402) 2 del PL3 SM010016380 (FBMA-L11-322513-201LMA40T)	2010-0617	to DVT
2	change bead to jump	6 layers change to 8 layers, so change bead to jump	0.1	51	del PL6 SM010016380 (FBMA-L11-322513-201LMA40T)	2010-0617	to DVT
3	change bead to jump	6 layers change to 8 layers, so change bead to jump	0.1	52	1 del PC70 SE074561K80 (S CER CAP 560P 50V K X7R 0402) 2 del PL9 SM010016380 (FBMA-L11-322513-201LMA40T)	2010-0617	to DVT
4	change bead to jump	6 layers change to 8 layers, so change bead to jump	0.1	53	1 del PC81 SE074561K80 (S CER CAP 560P 50V K X7R 0402) 2 del PL11 SM010020720 (FBMA-L18-453215-900LMA90T)	2010-0617	to DVT
5	change bead to jump	6 layers change to 8 layers, so change bead to jump	0.1	54	1 del PC89 SE074561K80 (S CER CAP 560P 50V K X7R 0402) 2 del PL13 SM010016380 (FBMA-L11-322513-201LMA40T)	2010-0617	to DVT
6	change main souce	cost down	0.1	54	Chnage PQ36 from SB000008L80(S TR SI7686DP-T1-E3 IN POWERPAK S08) to SB00000HL00(S TR TPCA8030-H 1N SOP-ADV) change PQ37 from SB000009F80(S TR AO4456 1N S08) to SB00000GL00(S TR TPCA8028-H 1N SOP ADVANCE) Del PQ38 SB000009F80(S TR AO4456 1N S08)	2010-0617	to DVT
7	reduce components quantity	cost down	0.1	53	Chnage PR104 from SD014100080(S RES 1/10W 100 +-5% 0603) to SD013100080 (S RES 1/10W 100 +-1% 0603)	2010-0624	to DVT
8	reduce components quantity	cost down	0.1	52	Chnage PR94 from SD014100080(S RES 1/10W 100 +-5% 0603) to SD013100080 (S RES 1/10W 100 +-1% 0603)	2010-0624	to DVT
9	change main souce	cost down	0.1	51	Chnage PQ15, PQ17 from SB00000DL00(S TR AO4407A 1P S08) to SB00000DJ10 (S TR AO4435L 1P S08)	2010-0624	to DVT
10	change main souce	cost down	0.1	51	Chnage PQ27 from SB00000CG00(S TR AO4466 1N S08) to SB000009580 (S TR AO4468 1N S08)	2010-0624	to DVT
11	change main souce	cost down	0.1	50	Chnage PQ9 from SB00000AJ00(S TR AO47I2 1N S08) to SB000009580 (S TR AO4468 1N S08)	2010-0624	to DVT
12	adjust OCP setting	Because Rds(on) change to 22m(MAX) and 17.4m(TYP) ohm of low side MOS, so change OCP setting	0.1	50	Chnage PR31 from SD034105380(S RES 1/16W 105K +-1% 0402) to SD034127380 (S RES 1/16W 127K +-1% 0402)	2010-0624	to DVT
13	change main souce	ISL62881C has hang up issue, so change to ISL62881.	0.2	54	Chnage PU8 from SA000043N00(S IC ISL62881CHRZ-T QFN 28P PWM) to SA000030200 (S IC ISL62881HRZ-T QFN 28P PWM)	2010-0713	to DVT
14	adjust resistance value	adjust resistance value for ISL62881	0.2	54	Chnage PR113 from SD034750180(S RES 1/16W 7.5K +-1% 0402) to SD034226280 (S RES 1/16W 22.6K +-1% 0402)	2010-0713	to DVT
15	adjust resistance value	adjust resistance value for ISL62881	0.2	54	Chnage PR121 from SD034287180(S RES 1/16W 2.87K +-1% 0402) to SD034866180 (S RES 1/16W 8.66K +-1% 0402)	2010-0713	to DVT
16	adjust resistance value	adjust resistance value for ISL62881	0.2	54	Chnage PR130 from SD000009380(S RES 1/16W 562 +-1% 0402) to SD00000JB80 (S RES 1/16W 1.69K +-1% 0402)	2010-0713	to DVT
17	add resistance	pop resistance for ISL62881	0.2	54	add PR136 SD034825A80(S RES 1/16W 82.5 +-1% 0402)	2010-0713	to DVT
18	add cup.	pop Cup. for ISL62881	0.2	54	add PC110 SE076103K80(S CER CAP .01U 16V K X7R 0402)	2010-0713	to DVT
19	adjust capacitor	Because ME height limit, so change to 8 height capacitor.	0.2	55	Chnage PC116 from SF22004M210(S ELE CAP 220U 25V M 8X10.2 CE-AX) to SF000000S80 (S ELE CAP 100U 25V M 6.3X7.7 CE-LX)	2010-0713	to DVT
20	add cup.	Because ME height limit, so add an 8 height capacitor.	0.2	55	Add PC135 SF000000S80 (S ELE CAP 100U 25V M 6.3X7.7 CE-LX)	2010-0713	to DVT
21	adjust resistance value	adjust resistance value for CPU loadline	0.2	55	Chnage PR179 and PR180 from SD014137380(S RES 1/10W 137K +-1% 0603) to SD014127380(S RES 1/10W 127K +-1% 0603)	2010-0715	to DVT
22	adjust resistance value	adjust resistance value for +5Valwp to 5.1V	0.2	50	Chnage PR28 from SD034300280(S RES 1/16W 30K +-1% 0402) to SD034309280(S RES 1/16W 30.9K +-1% 0402)	2010-0723	to DVT

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	EMI request reserve 0 ohm	EMI request reserve 0 ohm for EMI ISN test	0.3	43	change PJ16 to SD011000080(S RES 1/4W 0 +-5% 1206)	2010-0907	PVT
2	Add boost resister	EMI request add boost resister for EMI test	0.3	47	change PRI53 and PRI61 form SD013000080 to SD013220B80(S RES 1/10W 2.2 +-5% 0603)	2010-0907	PVT
3	Add snubber	EMI request add snubber for EMI test	0.3	47	Add PRI52 and PRI70 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC119 and PC129 SE025681K80(S CER CAP 680P 50V K X7R 0603)	2010-0907	PVT
4	Add boost circuit	Touch panel control board need high voltage 15V	0.3	49	Add FU10 SA00004DD00(S IC RT9293AGJ6 TSOT-23 6P BOOST) Add PL18 SHI00005P00(S INDUC_ 22UH +-20% NR3010T220M)	2010-0907	PVT
5	Add boost circuit	Touch panel control board need high voltage 15V	0.3	49	Add PD9 SCSSSM24A20(S DIO SSM24APT SMA-S) Add PQ44 SB00000DJ10(S TR AO4435L 1P SO8) Add PQ45 SB000006800(S TR 2N7002W T/R7 1N SOT-323)	2010-0907	PVT
6	Add boost circuit	Touch panel control board need high voltage 15V	0.3	49	Add PD10 SC1H751H010(S DIO CH751H-40PT SOD323) Add PR183, PR188 SD028100380(S RES 1/16W 100K +-5% 0402) Add PR185, PR187 SD028100280(S RES 1/16W 10K +-5% 0402)	2010-0907	PVT
7	Add boost circuit	Touch panel control board need high voltage 15V	0.3	49	Add PC136, PC140 SE076103K80(S CER CAP 0.01U 16V K X7R 0402) Add PC137 SE000000U00(S CER CAP 1U 16V K X5R 0402) Add PC139 SE102104K00(S CER CAP 0.1U 10V +-10% X7R 0402)	2010-0907	PVT
8	Add boost circuit	Touch panel control board need high voltage 15V	0.3	49	Add PR184 SD034143380(S RES 1/16W 143K +-1% 0402) Add PR186 SD034100180(S RES 1/16W 1K +-1% 0402)	2010-0907	PVT
9	Add boost circuit	Touch panel control board need high voltage 15V	0.3	49	Add PC138 SE000000QK00(S CER CAP 10U 25V K X5R 0805 H1.25)	2010-0907	PVT
10							
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1			0.1	48			
2			0.1	50			
3			0.1	51			
4			0.1	51			
5			0.1	52			
6			0.1	53			
7			0.1	46			
8			0.1	47			
9			0.1	52			
10			0.1	48			
11			0.1	52			
12			0.1	52			
13			0.2	46			
14			0.2	51			
15			0.2	52			
16			0.2	53			
17			0.2	52			
18			0.2	50			
19			0.2	55			
20			0.2	53			
21			0.2	55			
22			0.2	48			
23			0.2	52			

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